High-performance Multi-Bit Adder-Accumulators as Components of The ALU In Supercomputers

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Abstract

The fields of applications of multi-bit special-purpose processors for data processing in cyber-physical systems (CPS) are analyzed. Structures of multi-bit special-purpose processors (MSP) based on synchronized adders, which are used as components of arithmetic logic units (ALU) in multi-core vector and scalar supercomputers are classified. New efficient structures of MSPs, which process data given in mono binary and binary number systems, are proposed according to the criteria of maximum speed and reduced hardware complexity. The results of studies of the functional and structural, time and hardware characteristics of such MSPs are presented. Promising areas of their applications in scientific and industrial computerized systems are identified.

Keywords 1

Special-purpose processors, synchronized adders, cyber-physical systems, arithmetic logic units, binary number system, supercomputers.

1. Introduction

Nowadays, the creation and widespread use of modern supercomputers in various fields of knowledge and mathematics has made it possible to successfully solve complex mathematical and algorithmic problems offline, and in some cases online. Such supercomputers were developed by leading global companies (Intel, IBM, DEC, Motorola, ARM, SPARC, MIPS, PowerPC) [1-4]. Logical and computational operations in known supercomputers are usually implemented in binary arithmetic of the Rademacher number system. Supercomputers with 64-bit architecture, including EM64T, Turion 64, Xeon, Core2, Corei3, Corei5, Intel (IA-64 (Itanium)), UltraSPARC (Sun Microsystems), MIPS64 (MIPS) [4] can be applied in all branches of industry and in military field (special equipment).

Modern supercomputers, which include thousands of parallel processors, allow performing Teraflops (TFLOPS) of arithmetic and logical operations in one second in real time. Multi-bit supercomputers can also be used as system components of complex distributed CPS [5,6]. Through deep parallelization of computational operations, such supercomputers make it possible to solve multi-bit matrices in algebraic equations, simulate complex physical processes, perform pattern recognition and solve 3D digital holography problems. An important structural feature of well-known scalar and vector superprocessors is the large width of the processed digital data within the range of 128-2048 bits. This leads to the high level of relevance of the development of high-performance

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MSPs that execute arithmetic and logical operations of comparison, addition, multiplication, division, exponentiation and finding residues modulo in various number systems.

For the creation of such MSPs synchronized binary adders (SBA) can be beneficially used [7,8].

Recently, the problem of data crypto protection and cryptanalysis in computer networks and CPS has become relevant. Such data is also processed on the basis of multi-bit binary codes (1024-4096 bits) [9].

In particular, efficient and fast-acting solutions to such problems are needed in the conditions of military operations and modern information front, for example, data reprogramming of the functions of drones, missiles, unmanned aerial vehicles, ground launchers and high-performance processors of air defense systems.

A promising solution to these problems and applied data problems is the development and application of a new class of MSP based on binary arithmetic and synchronized binary adders (SBA) [10]. An example of such solutions is the development and use of multi-bit carry-look-ahead adders [11,12] and adder-accumulators [13] as components of ALU in supercomputers. Such SBAs are important components of multi-bit high-performance parallel and flow multipliers [12].

2. Related works

Multi-bit adder-accumulators are the basic components of ALUs of supercomputers. The main criterion of such components is the maximum speed of performing addition of multi-bit binary numbers, which determines the corresponding performance of supercomputer cores.

In [1-5,11,24], structural microelectronic implementations of classic combinational adders and adder-accumulators built on the basis of binary arithmetic were presented. The main shortcoming that does not allow significantly increasing the speed of such components in modern computer systems and superprocessors is the use of binary arithmetic, which involves ripple-carry overs between bits, which is a particularly negative factor in increasing the speed of multi-bit computing devices.

A structure of a single-bit binary full adder was shown in [7], in which the delay of ripple carry overs (C_{out}) is 2 clock cycles, and generation of the sum bit (S_i) is 6 clock cycles (Fig. 1).

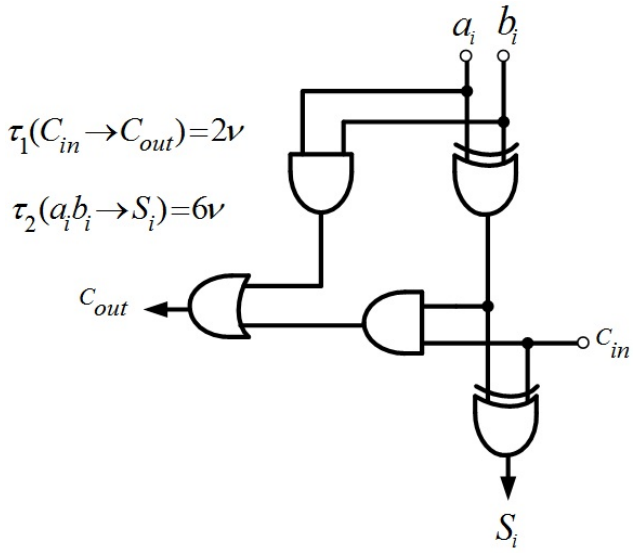


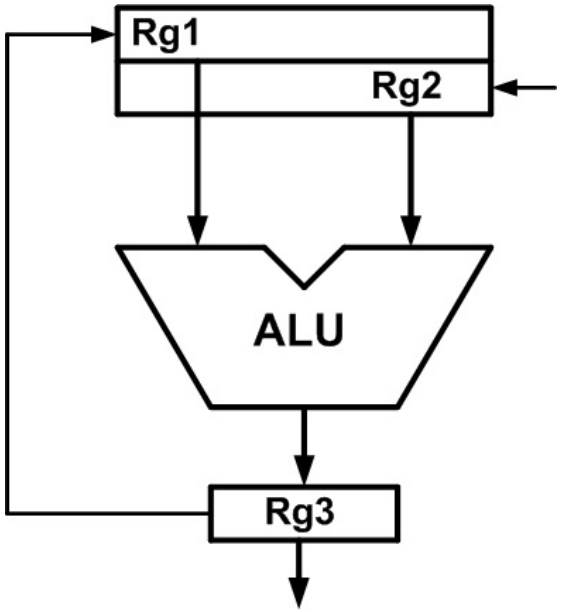
Figure 1: Microelectronic structure of a single-bit binary full adder

For example, when performing addition of two n-bit mono binary codes (MBC), signals are delayed in the computing device, respectively, by n clock cycles. That is, performing an addition operation with classic multi-bit binary adders (MBA) with direct information inputs and outputs, the register capacity of ALU of supercomputer core is from 128 to 2048 bits and the signal delay is from 256 to 4096 clock cycles, respectively.

At the same time, the relevant problem, which is presented in this article, is the development of improved structural solutions of adder-accumulators, which allow increasing the speed by 1-2 orders compared to known structures, according to the proposed binary arithmetic, which does not include ripple-carry overs, when performing addition operations and accumulation of the sums of binary codes. A deep comparative analysis of the proposed structures in relation to the classical ones is presented by the authors in [12,15,17].

3. Criteria and system characteristics of the synchronized ALU components of multi-bit supercomputers

Synchronized ALU components of supercomputer cores are memory registers and adder matrices (fig.2) [14,12,15].



System characteristics of combinational components of ALU:

1. $S_k = \sum_{i=1}^{n} X_i + \sum_{j=1}^{m} Y_j$;
2. $\tau = \sum_{j=1}^{m} \tau_j$;
3. $f_j = \sum_{i=1}^{n} \beta_i \times f_{input} + \sum_{i=1}^{m} \lambda_i \times f_{output}$;
4. $A_{\Pi} = \sum_{i=1}^{n} A_i$;
5. $A_{\Pi} = \sum_{j=1}^{m} \sum_{i=1}^{n} A_{ij}$.

Figure 2: A typical structure of the ALU of a computer core

The main system characteristics of the ALU matrix components are the following ones:

1. S_K – is determined by the total number of inputs/outputs of the microelectronic structure according to Quine's criterion;

2. τ – time complexity is determined by the total number of clock cycles of signal delay in the longest chain of logical or functional series connected components between the corresponding inputs/outputs of the device, where m is the number of series connected components; t_j –signal delay in each j-th component, υ – a number of clock cycles;

3. f_j –functional completeness of the device inputs/outputs, which is determined by the overall estimate, where f_j is the functional and informational characteristic of the device structure; B, J are the information coefficients of the input/output functions; m, n – the number of inputs and outputs; f_{input}, f_{output} – functions of inputs/outputs, e.g., input/output channel (x/y), input/output buses (n/m), sync input, crystal selection (c/s), power supply (+/-);

4. A – hardware complexity of the device, which is calculated as the total number of logic elements and gates in the microelectronic structure of the devices, where A_{Π} is the overall estimate of the hardware complexity, i, j, k are the types of components or levels of the device structure m, n, l.

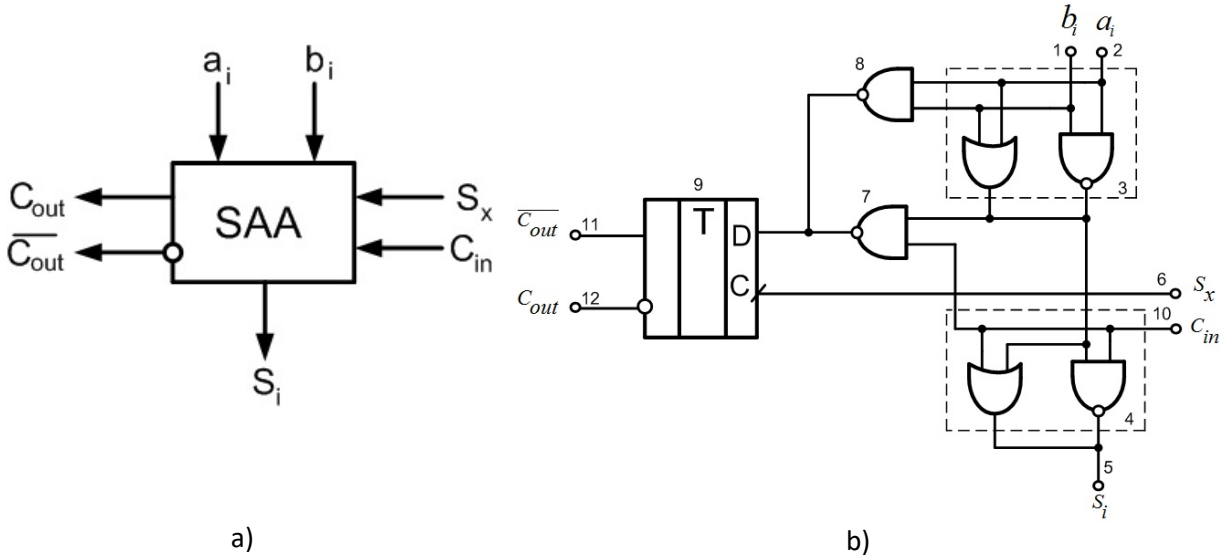
4. Functional structures and circuitry of single-bit synchronized binary adders

A functional feature of the SBA is the ability to store bits of sum (S_i) and carry (C_{out}) until the clock cycle of their use by the MSP in the microcycles of streaming data processing algorithms.

In microelectronics, well-known synchronized logic elements (AND, OR, NAND, NOR, XOR, NOT) and triggers of RS, D, T and JK types are used as components of special-purpose processors (SP) [7,8].

At the same time, single-bit SBA and multi-bit adders, which are characterized by minimax characteristics of speed and hardware complexity, are not fully presented and studied nowadays in literature in the field of computer circuitry and microelectronics.

Fig. 3 shows the developed functional and microelectronic structures of a single-bit synchronized adder-accumulator (SAA) based on a single-bit full binary adder [10]. They are characterized by enhanced functionality compared to known structures.



a) b)

Figure 3: Functional structure of SAA (a), microelectronic structure of SAA (b)

SAA includes data inputs (a_i,b_i,C_{in},S_x) and outputs (S_i,C_{out}, $\overline{C_{out}}$) and consists of two components, i.e., a combinational adder and D- trigger.

The combinational binary adder contains two series connected logic elements XOR (3,4), which are implemented on the basis of the proposed logical function "Exclusive AND" according to the expression:

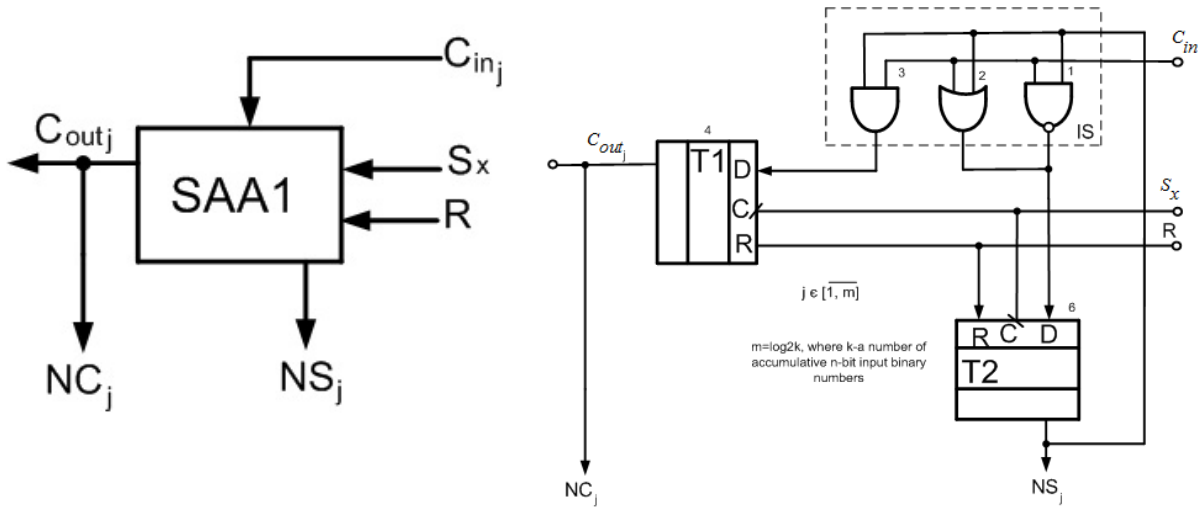
Parallel generation of the output paraphase (qubit) ripple carry (C_{out}, $\overline{C_{out}}$) is implemented on the direct and inverse outputs of the D-trigger. Thus, the given structure of the SHAA allows us to generate the data output of ($S_i = a_i + b_i$) sum and store the qubits of the output ripple carry-overs, which makes it possible to apply it in the structures of quantum computers [16].

Such a SAA has the following system characteristics:

1. Structural complexity of an adder: $S_k = 4+3 = 7$.
2. Input/output speed parameters: $\tau_1(a_i b_i \to S_i) = 2\nu$; $\tau_2(a_i b_i \to 3 \to 7 \to 9 \to C_{out}) = 4\nu$; $\tau_3(a_i b_i \to 8 \to 9 \to C_{out}) = 3\nu$; $\tau_4(C_{in} \to 7 \to 9 \to C_{out}) = 4\nu$; $\tau_5(S_x \to 9 \to C_{out}) = 2\nu$.
3. f_i – functional completeness of inputs/outputs: $f_i = 4+(2+(1\times 2)) = 4+4 = 8$.
4. A – hardware complexity: $A = A_{SAA} + A_T = 6+2 = 8$ (logical elements).

The described structure of the SAA is not characterized by the functional completeness for its use as a component of the adder-accumulator.

Fig. 4 shows the developed functional and microelectronic structures of a single-bit synchronized adder-accumulator (SAA1) based on a single-bit half binary adder, which has enhanced functionality compared to known structures [10].



a) b)

Figure 4: Functional structure of a single-bit synchronized half adder-accumulator (SAA1) (a), microelectronic structure of a single-bit synchronized half adder-accumulator (SAA1) (b)

SAA1 includes data inputs: C_{inj} – ripple carry, S_x – synchronization, R – reset of D-triggers to the zero state; data outputs (C_{outj}, NC_j, NS_j), and consists of a single-bit increment adder and two D-triggers. This SAA1 has the following system characteristics:

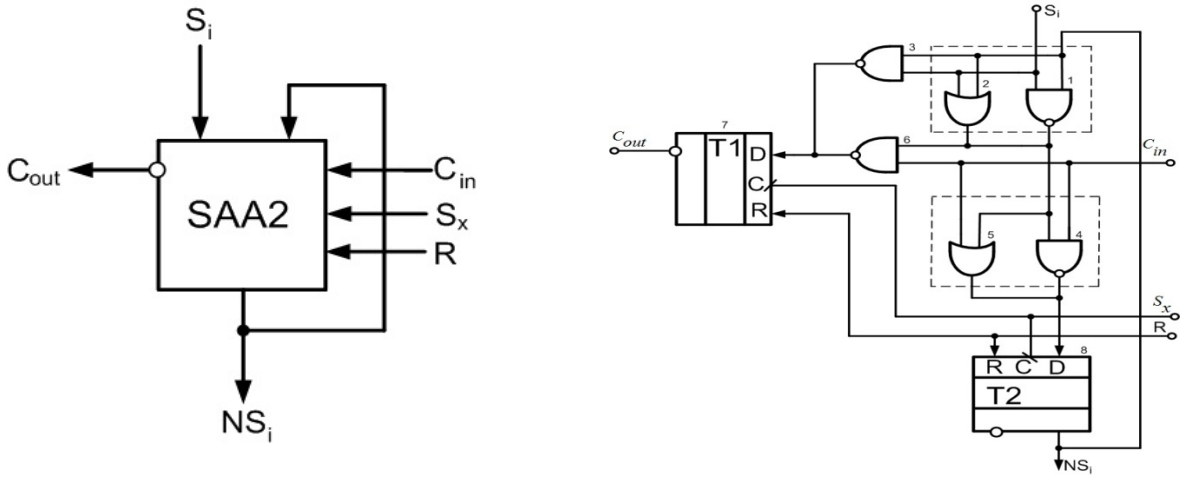
1. Structural complexity of the adder: $S_k = 3+3 = 6$.

2. Input and output speed parameters: $\tau_1(C_{in} \to 3 \to T1 \to C_{out}) = 3\nu$; $\tau_2(C_{in} \to 1 \to T2 \to NS_j) = 3\nu$; $\tau_3(S_x \to T1) = 2\nu$.

3. f_i - input and output functional completeness: $f_i = 3+3 = 6$.

4. A – hardware complexity: $A = A_{SAA1} + 2A_T = 3+4 = 7$ (logical elements).

The functional and developed microelectronic structures of a single-bit full adder-accumulator (SAA2) based on a single-bit full binary combinational adder are presented in Fig. 5.



a) b)

Figure 5: Functional structure of a single-bit full adder-accumulator (SAA2) (a), microelectronic structure of a single-bit full adder-accumulator (SAA2) (b)

SAA2 includes data inputs and outputs: S_i – data bit; C_{in} – ripple carry input; S_x –synchronization; R – reset of D-triggers to the zero state; C_{out} – the output of the ripple carry; NS_i – the output of the accumulated sum.

The structure of such SAA2 includes a single-bit binary full adder based on two series connected XOR logic elements (indicated by dashed borders) and two D-triggers that store the ripple carry bit (C_{out}) and the accumulated sum bit (NS_i).

Such SAA2 has the following system characteristics:

1. Structural complexity of the adder: $S_k = 4+2 = 6$.
2. Input and output speed parameters: $\tau_1(S_i \to 1 \to 4 \to T2 \to NS_j) = 4\nu$; $\tau_2(S_i \to 1 \to 6 \to T1 \to C_{out}) = 4\nu$; $\tau_3(C_{in} \to 6 \to T1) = 3\nu$; $\tau_4(C_{in} \to 4 \to T2) = 3\nu$.
3. f_i - input and output functional completeness: $f_i = 4+2 = 6$.
4. A – hardware complexity: $A = A_{SAA2} + 2A_T = 6+4 = 10$ (logical elements).

Adder-accumulators SAA1 and SAA2 are the basic components of multi-bit synchronized adder-accumulators (MSAA), which are functional special-purpose processors of multi-bit supercomputer cores. Such components are prioritized by the characteristics of maximum speed, when solving complex computational problems including determination of one-dimensional and two-dimensional sums.

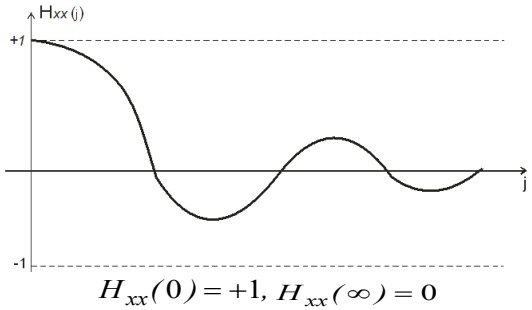
5. Fields of applications and circuit structure of multi-bit synchronized adder-accumulators (MSAA)

MSAAs are widely used as processor components for statistical, correlation, spectral, and entropy data processing [15]. When calculating these characteristics, the following algorithms are used:

$$M_x = \frac{1}{n}\sum_{i=1}^{n} X_i \; ; M_j = \frac{1}{n}\sum_{i=1+j}^{n+j} X_{i+j} \; ; \quad M_v = \frac{1}{n}\sum_{i=1+j}^{n+j} V_{i-j} X_{i+j} \; ; \quad D_x = \frac{1}{n}\sum_{i=1}^{n} (X_i - M_x)^2 \; , \qquad (1)$$

where, $i \in \overline{1,n}$ - sample size; $j \in \overline{0,m}$ - discrete shift of data array, M_x, M_j, M_v - respectively, selective, sliding and weighted mathematical expectations, which are calculated according to the expressions, $(X_i - M_x) = \overset{\circ}{X}_i$ - centered digital data; D_x, δ_x - variance and standard deviation, respectively.

In Figures 6 – 12, the analytics and asymptotics of basic autocorrelation functions (ACF), which include multiple sum accumulation operations and are widely used in practice for correlation analysis and pattern recognition.

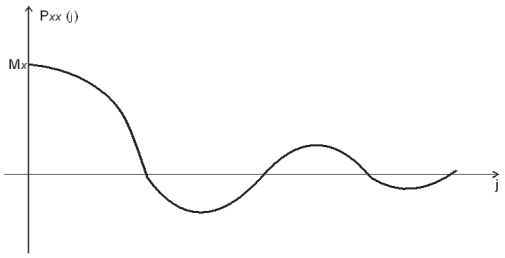


$$H_{xx}(0) = +1, \; H_{xx}(\infty) = 0$$

$$H_{xx}(j) = \frac{1}{n}\sum_{i=1}^{n} sign\, \overset{o}{x}_i \cdot sign\, \overset{o}{x}_{i+j}$$

$$sign\, \overset{o}{x}_i = \begin{cases} +1, \overset{o}{x}_i \geq 0 \\ -1, \overset{o}{x}_i < 0 \end{cases}$$

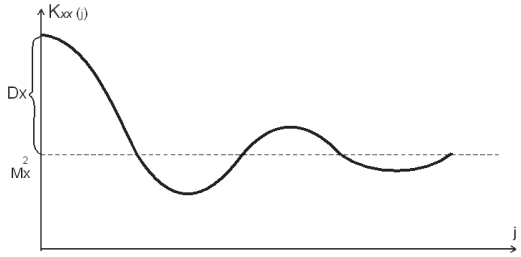
Figure 6: Sign ACF



$$P_{xx}(j) = \frac{1}{n}\sum_{i=1}^{n} \overset{o}{x}_i \cdot sign\, \overset{o}{x}_{i+j}$$

$$P_{xx}(0) = M_x,\ P_{xx}(\infty) = 0$$

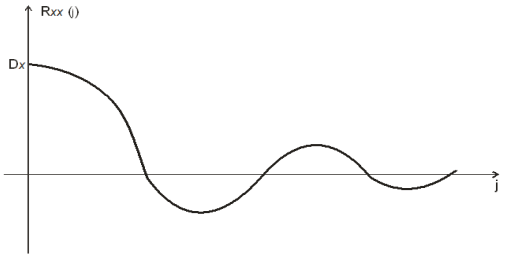
Figure 7: Relay ACF



$$K_{xx}(j) = \frac{1}{n}\sum_{i=1}^{n} x_i \cdot x_{i+j}$$

$$K_{xx}(0) = D_x + M_x^2,\ K_{xx}(\infty) = M_x^2$$

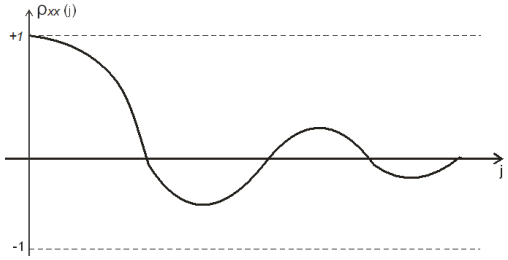
Figure 8: Covariance ACF



$$R_{xx}(j) = \frac{1}{n}\sum_{i=1}^{n} \overset{o}{x}_i \cdot \overset{o}{x}_{i+j}$$

$$R_{xx}(0) = D_x,\ R_{xx}(\infty) = 0$$

Figure 9: Correlation ACF

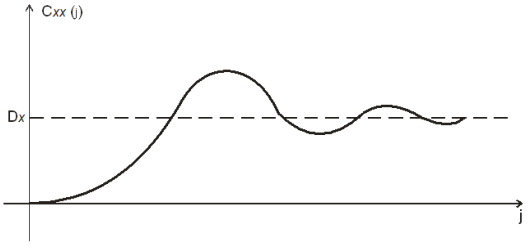


$$\rho_{xx}(j) = \frac{R_{xx}(j)}{D_x},$$

$$D_x = \frac{1}{n}\sum_{i=1}^{n}(x_i - M_x)^2$$

$$\rho_{xx}(0) = +1,\ \rho_{xx}(\infty) = 0$$

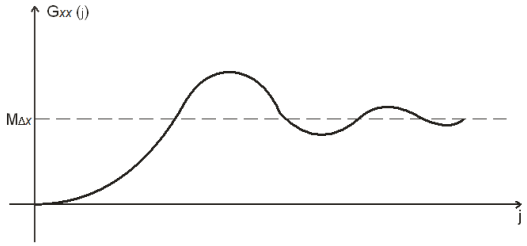
Figure 10: Normalized ACF



$$C_{xx}(0) = 0,\ C_{xx}(\infty) = D_x$$

$$C_{xx}(j) = \frac{1}{n}\sum_{i=1}^{n}(x_i - x_{i+j})^2$$

Figure 11: Structural ACF



$$G_{xx}(j) = \frac{1}{n} \cdot \sum_{i=1}^{n} \left| x_i - x_{i+j} \right|$$

$$G_{xx}(0) = 0,\ G_{xx}(\infty) = M_x$$

Figure 12: Modular ACF

Determining the spectrum of a random process looks as follows:

$$S_w = \frac{1}{m} \sum_{j=1}^{M} \rho_{xx}(j) \times w_j \times e^{-\alpha j} \quad , \tag{2}$$

where $\rho_{xx}(j)$ - normalized autocorrelation function; w – a type of orthogonal basis function: F - Fourier function; H – Haar function; R – Rademacher function; W – Walsh function; C – Crestenson function; and others [17].

Euclidean and Hamming distances are estimated in pattern recognition based on RGB color image processing [15] according to the following expressions:

1. Euclidean distance:

$$d(i,j) = \sqrt{\sum (x_i - x_j)^2} \ ; \tag{3}$$

where, x_i, x_j - image features.

2. Manhattan distance:

$$d_m(i,j) = \sum_{i=1}^{M} \sum_{j=1}^{N} \left| x_i - y_j \right| . \tag{4}$$

3. Static distance:

$$d_S(i,j) = (\sum_{i=1}^{M} \sum_{j=1}^{N} \left| x_i - y_j \right|^{P})^{\frac{1}{2}} , P \to \infty . \tag{5}$$

4. Chebyshev distance:

$$d_c(i,j) = \max \sum \left| x_i - x_j \right| . \tag{6}$$

5. The distance of the least (D_1) and most (D_2) remote cluster neighbors:

$$D_1(A,B) = \min \left\{ d_{ij} \right\} ;\ i \to A ;\ j \to B ;\ D_2(A,B) = \max \left\{ d_{ij} \right\} . \tag{7}$$

6. Pairwise average:

$$D_S(A,B) = \frac{1}{|A| \times |B|} \sum_{i=1}^{A} \sum_{j=1}^{B} d_S(i,j) . \tag{8}$$

7. Centroid method:

$$D_S(A,B) = (d_S(ic,jc)) , \tag{9}$$

where, ic, jc - centroids of image clusters A and B.

8. Ward's method:

$$D_S(A,B) = d_e / (|A| \times |B|) , \tag{10}$$

where, $d_e = \sqrt{\sum (x_k - \bar{x})^2}$, x_k - pixel coordinates, $\bar{x}$ - mathematical expectation of coordinates.

Calculation of the cumulative histogram of a two-dimensional color image as the sum of the probabilities of separate colors is as follows [18,19]:

$$V_1(S) = \sum_{i \in n,S}^{n,S} P_2(i). \tag{11}$$

Probabilistic entropy is estimated according to C. Shannon in the following way [20]:

$$H_k = -k \sum_{j=0}^{S} p_j \log_k p_j, \tag{12}$$

where, H_x - entropy estimate; k – coefficient of the algorithm base (2,10,e,..); P_i - the probability of a random process.

For each image segment, the variance of the deviations of $P_i(i)$ and $P_2(i)$ values from the arithmetic mean value is calculated as an iterative procedure.

The given list of analytical expressions and corresponding algorithms for digital data processing allow us to solve the important problems of applied mathematics and microelectronic circuits to provide the conditions for minimax criterion of speed and hardware complexity of MSAA structures.

The developed MSAA microelectronic circuitry (Fig. 13) is implemented on the basis of the series connection of single-bit full SAAs1 (Fig. 4) and half SAAs2 (Fig. 4). The n-bit group of such an adder includes SAAs2, and more significant bits contain SAAs1 [21].

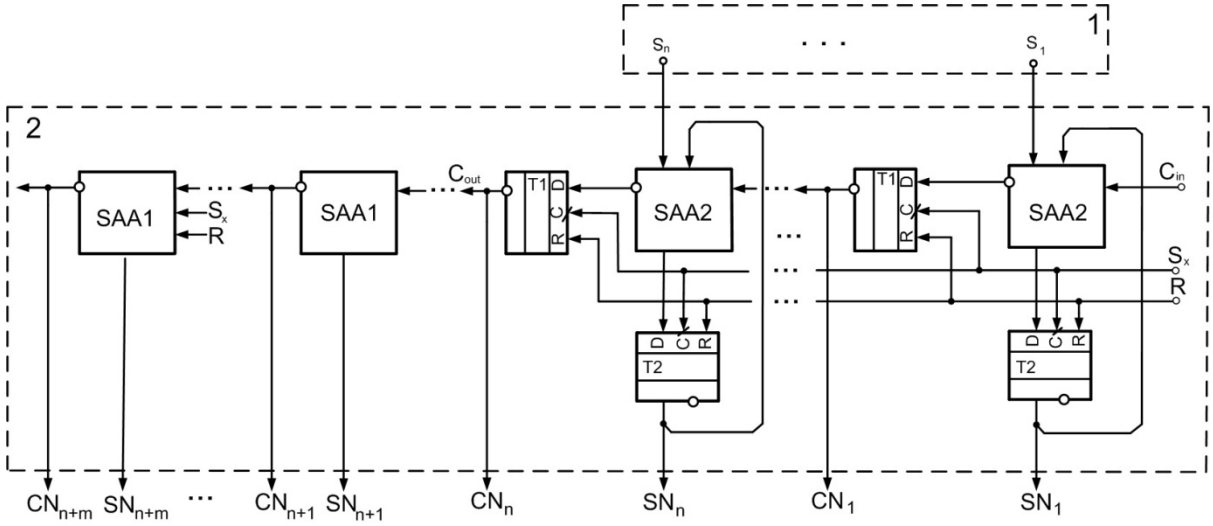


Figure 13: Functional structure of MSAA

The application of such MSAA as a component of MSP is presented in Fig. 13. Addition and accumulation of the n-sum of k-bit binary numbers is performed in each microcycle during 4 clock cycles, regardless of their bitness.

For example, when adding n=256 of k-bit numbers, the total number of microcycles is $N_1 = 4n = 1024$, that is, in comparison with known devices of this class, in which ripple carry-overs are available in each microcycle, the total number of microcycles for the considered example, with the number capacity of $k = (128 \div 4096)$, the signal delay in each microcycle, respectively, is $N_2 = 256 \times ([512 \div 8192)] + \log_2 256 = (133120 \div 2099200)$. That is, the performance of the improved MSAA, compared to the known one, increases by $k_{sb} = N_1 / N_2 = (133120 \div 2099200) / 1024 = (130 \div 2050)$ times. As the capacity of the accumulated binary numbers increases, the performance increases by 1-3 orders.

It should be noted that the result obtained at the output of such an adder-accumulator is presented by a binary code of $\dot{C}_n \dot{S}_n$ type:

$$\dot{C}_n \dot{S}_n, ..., \dot{C}_j \dot{S}_j, ..., \dot{C}_1 \dot{S}_1, \tag{13}$$

where, $\dot{C}_j$ is a bit of a ripple carry, $\dot{S}_j$ – a bit of a sum in j-th position of the MSAA output code, correspondingly.

Theoretical background and examples of computational operations on binary codes are given in Section 4 of this paper.

In case, when the results of accumulating the sum of many binary numbers are practically used in mono binary codes, the resulting binary code is converted into a mono binary code using a multi-bit binary carry-look-ahead adder [22]. The functional structure of such a multi-bit carry-look-ahead adder is shown in Fig. 14. The delay of ripple carry signals in the structure of a multi-bit carry-look-ahead adder in the first and final modules is 2 clock cycles, and in other modules it is 1 clock cycle.

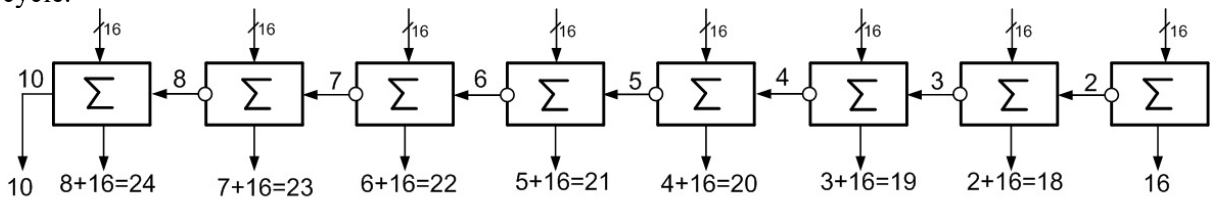


Figure 14: Functional structure of a multi-bit carry-look-ahead adder

Each component of a multi-bit carry-look-ahead adder (∑) in Fig. 14 is presented by the microelectronic structure of a multi-bit binary adder, which is shown in Fig. 15. An example of a 4-bit functional structure of the carry-look-ahead adder, which is a component of the decoder of the MSAA output binary code, is shown in Fig. 15 [22, 23].

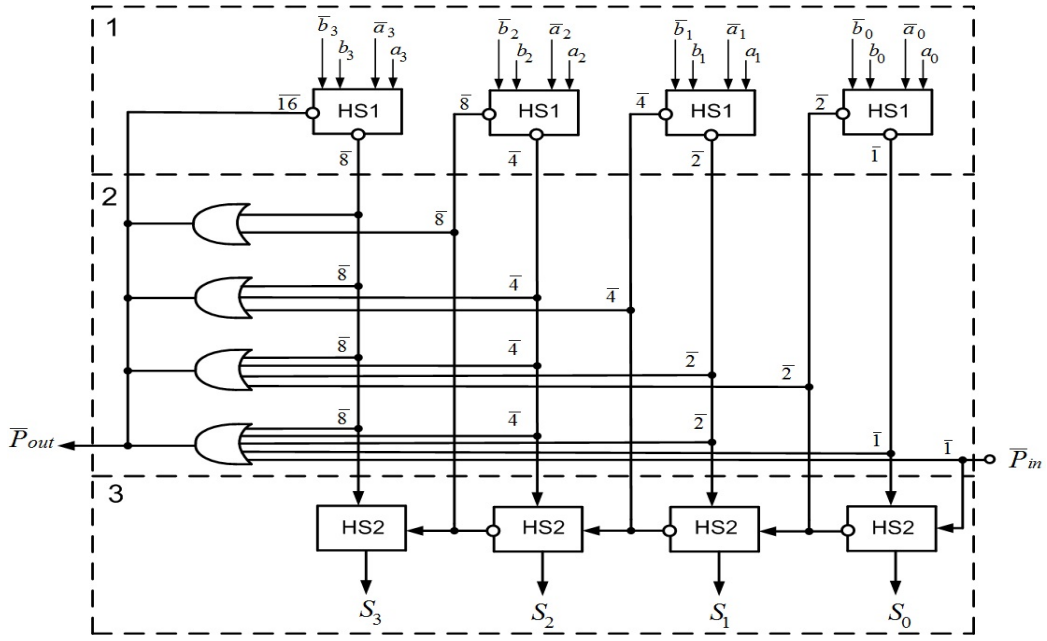


Figure 15: Functional structure of a 4-bit carry-look-ahead adder

Fig. 16 shows the microelectronic structures of the adder-accumulator components (HS1, HS2).

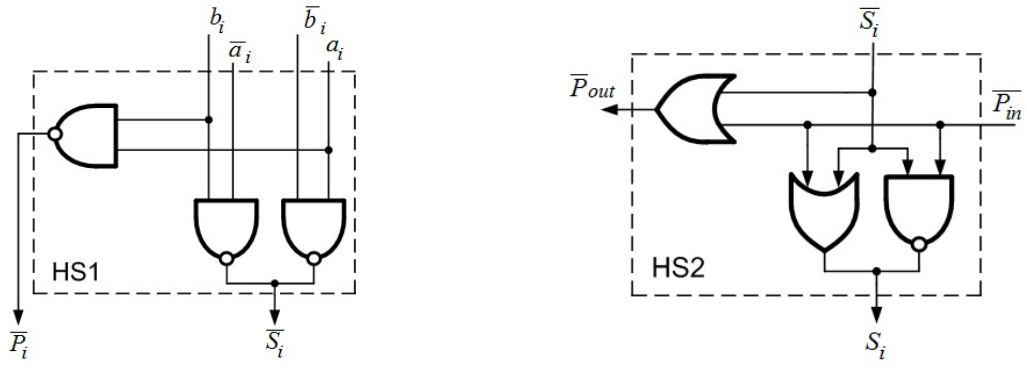


Figure 16: Microelectronic structures (HS1, HS2) as the components of a carry-look-ahead adder

The performance of such components of the binary code decoder [22] is 2 clock cycles, respectively. That is, when the capacity of the input binary code is n=256, the total signal delay is 48 clock cycles.

According to the example shown in Fig. 6, it can be seen that when the binary number position is (k=128) and taking into account that the sequentially generated bits of ripple carry (C_j) and bit sums (S_j) are to be converted, then the output mono binary code of the accumulated sum is generated in $2 \times 24 = 48$ clock cycles. That is, increasing the speed of accumulating the sum by multi-bit adder-accumulators (MAA) and presenting calculation results by mono binary code is, respectively, $k_{sm} = (133120 \div 48)/1024 = 130$ times. In this case, the MAA performance improving coefficient practically decreases by 0.01%.

More in-depth studies of the system performance characteristics and hardware complexity of this class of microelectronic binary accumulative codes should take into account the existing circuit design technologies developed by well-known companies (Texas Instruments, Analog Devices), which is beyond the scope of this work.

6. Application of MSAA as the ALU component of multi-bit vector and scalar supercomputers

Binary arithmetic of the ALU in multi-bit supercomputer is based on registration of bits of sum ($\dot{S}_j$) and bits of ripple carry-overs ($\dot{C}_j$) in each position.

An example of generating a binary code as a result of adding two mono binary codes (x and y) is presented in the following graph.

$$\begin{array}{l} x = (\quad a_{n-1}, \quad \ldots \quad , a_i, \quad \ldots \quad , a_1, \quad a_0 \quad) \\ +y = (\quad b_{n-1}, \quad \ldots \quad , b_i, \quad \ldots \quad , b_1, \quad b_0 \quad) \\ \hline \dot{d} = (\quad \dot{C}_n < \dot{S}_{n-1}, \ \ldots \ , \dot{C}_{i+1} < \dot{S}_i, \ \ldots \ \dot{C}_2 < \dot{S}_1, \ \dot{C}_1 < \dot{S}_0) \end{array}, \qquad (14)$$

where, $x = \sum_{i=0}^{n-1} a_i \cdot 2^i;\ y = \sum_{i=0}^{n-1} b_i \cdot 2^i;\ \dot{d} = \sum_{i=0}^{n-1} S_i \cdot 2^i + \sum_{i=0}^{n-1} C_{i+1} \cdot 2^i.$

Thus, each position of a binary number is presented by two bits that correspond to quaternary arithmetic according to Table 1.

Notation of a binary code (BC) position in binary arithmetic

Table 1

Truth table of binary code

$\dot{C}_{i+1}$	$\dot{S}_i$	$\dot{d}_i$
0	0	0
0	1	S
1	0	2S
1	1	3S

A simplified demonstration of the operation of generating a binary code is shown as an example of adding two 8-bit Fermat and Mersenne numbers, which correspond to the following numbers in the decimal and mono binary number systems $255_{(10)} = 11111111_{(2)}$; $129_{(10)} = 10000001_{(2)}$. Let us notate these numbers as a binary code and perform the operation of addition on them.

$$\begin{array}{l} \dot{x} = (0<1, \quad \ldots \quad ,0<1, \quad \ldots \quad ,0<1, \quad 0<1) \\ +\dot{y} = (0<1, \quad \ldots \quad ,0<0, \quad \ldots \quad ,0<0, \quad 0<1) \\ \hline \dot{d} = \quad (1<1, \quad \ldots \quad ,1<0, \quad \ldots \quad ,1<0, \quad 1<0) \end{array}.$$

Such an operation of adding two mono binary codes (MBC) presented by BC ($\dot{x}$ and $\dot{y}$) and their sum ($\dot{d}$) is implemented by the following structure of an n-bit combinational adder based on single-bit half binary adders (HBA), which is shown in Fig. 17.

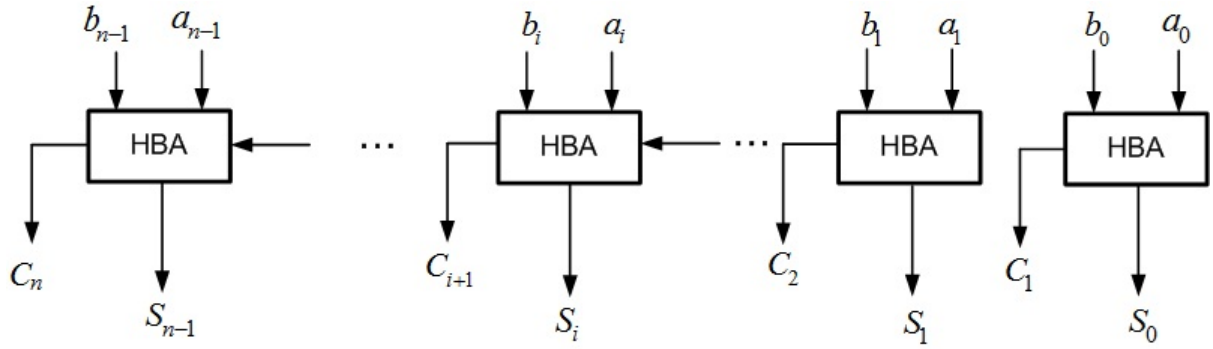


Figure 17: Structure of an n-bit binary adder for adding two n-bit mono binary codes at the output of which (n+1)-bit binary code is generated

N-bit binary adder whose structure is presented in Fig. 17, allows us to add two multi-bit binary mono codes in 1 clock cycle, regardless of the input code capacity.

The use of binary codes in the ALU structures of supercomputers makes it possible to increase the speed of calculations and the performance of digital data processing by 1-3 orders. Such computational operations on the data are implemented according to the analytical expressions presented in Section 3 (1-12). It is especially efficient when solving complex mathematical and algorithmic problems in the field of cryptography, holography and pattern recognition by processing images represented by RGB pixels of digital video cameras.

7. Conclusion

The proposed new functional and microelectronic structures of synchronized binary adders make it possible to significantly expand the scope of applications of multi-bit adders of digital data, and to increase their speed by 1-3 orders compared to known structures.

The presented theoretical and applied solutions of binary arithmetic significantly expand the possibilities of using ALU coprocessors in the computing environment of vector and scalar supercomputers.

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