

Speaker: Kyosuke Kageyama (Kindai University, Japan)

Biography: Kyosuke Kageyama received his B.E. degree from department of VLSI system design, and completed the first half of the M.E. program in department of electrical and electronic engineering from Ritsumeikan University, Shiga, Japan, in 2014 and 2016, respectively. He received the Ph.D. degree in department of electrical and electronic engineering from Ritsumeikan University, Shiga, Japan, in 2022. From 2016 to 2017, he was with Scientific Research Institute of Mie Prefectural Police Headquarters. From 2017 to 2019, he was with visiting scholar of Ritsumeikan University, Shiga, Japan. From 2019 to 2021, he was with Kyoto city Fire Department. From 2017 to 2022, he was with Japan Fire and Disaster Management Agency. Since 2022, he has been an Assistant Professor in the Department of Electrical, Electronic and Communication Engineering, Kindai University, Osaka, Japan, and he has been with visiting scholar of Ritsumeikan University, Shiga, Japan. His research interests include content addressable memory, SIMD processing architecture, visible light communication, image processing, and these applications. He is a member of the Institute of Electrical and Electronics Engineers (IEEE), the Information Processing Society of Japan (IPSJ), and the Institute of Electrical Engineers of Japan (IEEJ).

Title: Verification of Content Addressable Memory-based massive-parallel SIMD matrix core

Abstract: Recently, several multimedia applications, which are digital image compression, video compression, audio processing, and so on, have been implemented on mobile devices. In addition, Artificial Intelligence (AI) processing has grown rapidly. Therefore, mobile devices are necessitating the execution of large amounts of data. The processing core in a mobile device requires high performance, programmability, and versatility. Multimedia applications typically comprise repeated arithmetic and table-lookup coding operations. A Content Addressable Memory-based massive-parallel SIMD matrix core (CAMX) is proposed to increase the processing speed of both operations on a processing core. The CAMX serves as a CPU core accelerator for mobile devices. The CAMX supports massive parallel processing and is equipped with two content addressable memory modules and many processing elements. The CAMX has great performance, programmability, and versatility on mobile devices because it can handle logical, arithmetic, search, and shift operations in parallel. In this talk, the CAMX will be simulated basic calculation, encryption processing, and image processing.