SSD1363

Product Preview

320 x 160 Dot Matrix
OLED/PLED Segment/Common Driver with Controller

Appendix: IC Revision history of SSD1363 Specification

Version	Change Items	Effective Date
0.10	1st Release	07-Jan-2020

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TABLES

FIGURES

1 GENERAL DESCRIPTION

SSD1363 is a single-chip CMOS OLED/PLED driver with controller for organic / polymer light emitting diode dot-matrix graphic display system. It consists of 320 segments and 160 commons. This IC is designed for Common Cathode type OLED panel.

SSD1363 displays data directly from its internal 320 x 160 x 4 bits Graphic Display Data RAM (GDDRAM). Data/Commands are sent from general MCU through the hardware selectable I2C Interface, 6800-/8080-series compatible Parallel Interface or Serial Peripheral Interface.

The 256 steps contrast control and oscillator which embedded in SSD1363 reduces the number of external components. SSD1363 can be widely used in many applications such as set-top box, home appliance and industrial control panel.

2 FEATURES

- Resolution: 320 x 160 dot matrix panel
- Power supply
  - V_{DD} = 1.65V – 3.5V (MCU interface logic level & low voltage power supply)
  - V_{CC} = 8.0V – 18.0V (Panel driving power supply)
- Segment maximum source current: 500uA
- Common maximum sink current: 120mA
- 16 gray scale levels supported by embedded 320 x 160 x 4 bit SRAM display buffer
- Pin selectable MCU Interfaces:
  - 8/16 bits 6800/8080-series parallel Interface
  - 3/4 wire Serial Peripheral Interface
  - I2C Interface
- Internal or external I_{REF} selection
- RAM write synchronization signal
- Programmable Frame Rate and Multiplexing Ratio
- Row Re-mapping and Column Re-mapping
- Selectable Common current sinking mode:
  - Dual COM mode
  - Singe COM mode
- Support Cascade Mode
- 6-bit programmable Gray Scale Look Up Table
- On-Chip Oscillator
- Screen saving continuous scrolling function in both horizontal and vertical direction
- Screen saving infinite content scrolling function
- Power On Reset (POR)
- Chip layout for COG , COF
- Wide range of operating temperature: -40°C to 85°C

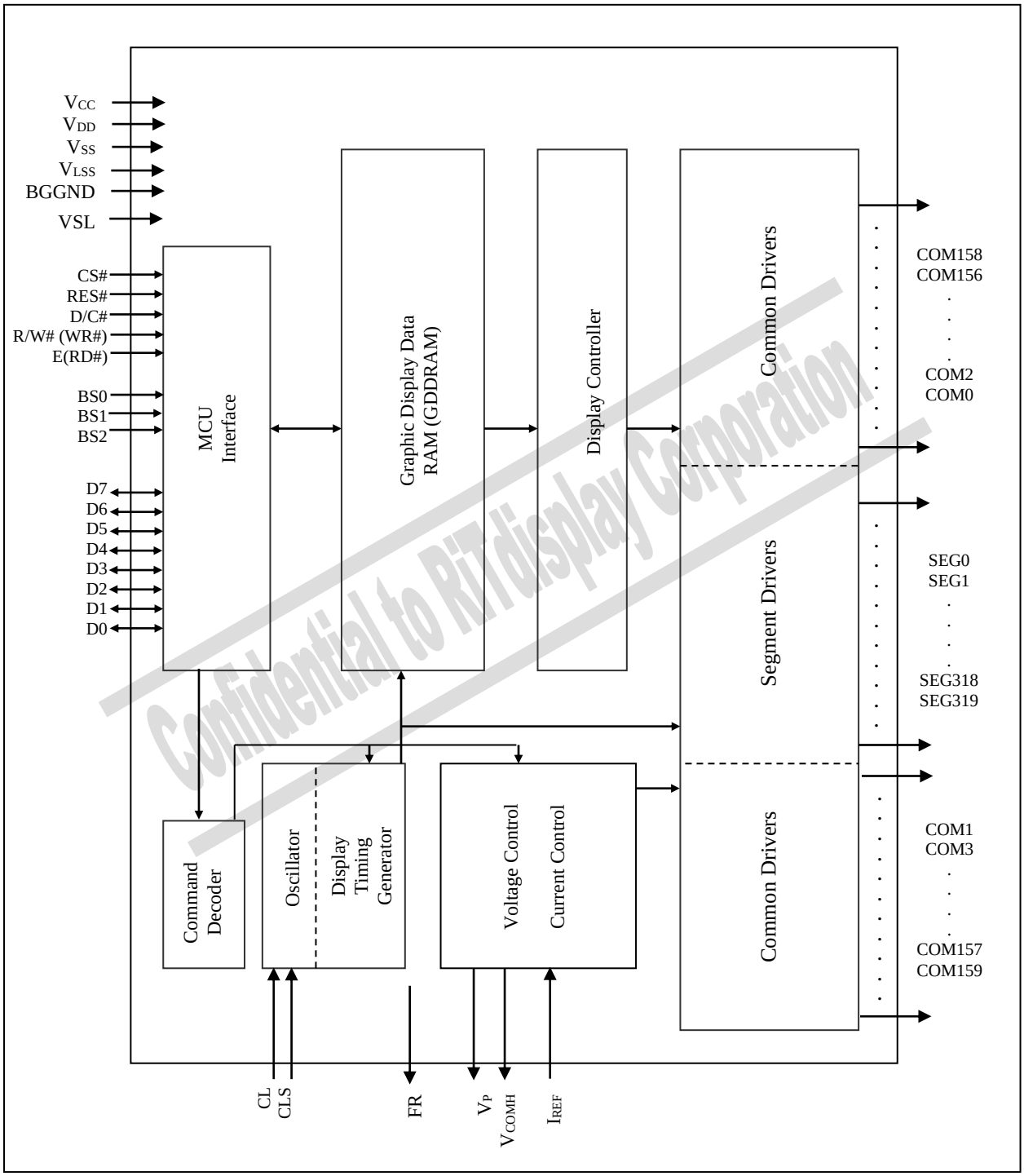
3 ORDERING INFORMATION

Table 3-1: Ordering Information

Ordering Part Number	SEG	COM	Package Form	Remark
SSD1363Z2	320	160	COG	○ Min SEG pad pitch : 25um ○ Min COM pad pitch : 27um ○ Min I/O pad pitch : 50um ○ Die thickness: 250um ○ Bump height: nominal 9um

4 BLOCK DIAGRAM

Figure 4-1: SSD1363 Block Diagram



5 PIN DESCRIPTION

Key:

I = Input	NC = Not Connected
O =Output	Pull LOW= connect to V_{LL} / Ground
I/O = Bi-directional (input/output)	Pull HIGH= connect to V_{LH} / V_{DD}
P = Power pin	

Table 5-1: Pin Description

Pin Name	Pin Type	Description
V_{DD}	P	Power supply pin for core logic operation. A capacitor should be connected between this pin and V_{SS}.
V_{CC}	P	Power supply for panel driving voltage. This is also the most positive power voltage supply pin. A capacitor should be connected between this pin and V_{SS}.
V_p	P	This pin is the segment pre-charge voltage reference pin. A capacitor can be connected between this pin and V_{SS} to improve visual performance. It can also be float per application. No external power supply is allowed to connect to this pin.
BGGND	P	Reserved pin. It must be connected to V_{SS}.
V_{SS}	P	Ground pin. It must be connected to external ground.
V_{LSS}	P	Analog system ground pin. It must be connected to external ground.
V_{SS1}	P	Reserved pin. It must be connected to V_{SS}.
VSL	P	This is segment voltage (output low level) reference pin. This pin has to be connected with resistor and diode to ground (details depends on application).
V_{COMH}	P	COM signal deselected voltage level. A capacitor should be connected between this pin and V_{SS}.
VBREF	O	This is a reserved pin. It should be kept NC.
V_{LH}	P	Logic high (same voltage level as V_{DD}) for internal connection of input and I/O pins. No need to connect to external power source.
V_{LL}	P	Logic low (same voltage level as V_{SS}) for internal connection of input and I/O pins. No need to connect to external ground.
BS[2:0]	I	MCU bus interface selection pins. Select appropriate logic setting as described in the following table. BS2, BS1 and BS0 are pin select. **Table 5-2: Bus Interface selection** BS[2:0] / Interface: 000 = 4 line SPI; 001 = 3 line SPI; 010 = I^2C; 100 = 8-bit 6800 parallel; 110 = 8-bit 8080 parallel **Note:** (1) 0 is connected to V_{LL} (2) 1 is connected to V_{LH}

Pin Name	Pin Type	Description
I_{REF}	I	This pin is the segment output current reference pin. I_{REF} is supplied externally. A resistor should be connected between this pin and V_{SS} to maintain the current around 10uA. It should be kept floating when internal I_{REF} is chosen by command setting.
CL_MS1	I	This is external clock input pin. When internal clock is enabled (i.e. HIGH in CLS pin), this pin is not used and should be connected to V_{LL}. When internal clock is disabled (i.e. LOW in CLS pin), this pin is the external clock source input pin.
CLS	I	This is internal clock enable pin. When it is pulled HIGH (i.e. connect to V_{LH}), internal clock is enabled. When it is pulled LOW (i.e. connect to V_{LL}), the internal clock is disabled; an external clock source must be connected to the CL pin for normal operation.
CS#	I	This pin is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CS# is pulled LOW (active LOW).
RES#	I	This pin is reset signal input. When the pin is pulled LOW, initialization of the chip is executed. Keep this pin pull HIGH during normal operation.
D/C#	I	This pin is Data/Command control pin connecting to the MCU. When the pin is pulled HIGH, the data at D[15:0] will be interpreted as data. When the pin is pulled LOW, the data at D[15:0] will be transferred to a command register. In I^2C mode, this pin acts as SA0 for slave address selection. When 3-wire serial interface is selected, this pin must be connected to V_{SS}.
R/W# (WR#)	I	This pin is read / write control input pin connecting to the MCU interface. When 6800 interface mode is selected, this pin will be used as Read/Write (R/W#) selection input. Read mode will be carried out when this pin is pulled HIGH and write mode when LOW. When 8080 interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled LOW and the chip is selected. When serial or I^2C interface is selected, this pin must be connected to V_{SS}.
E (RD#)	I	This pin is MCU interface input. When 6800 interface mode is selected, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled HIGH and the chip is selected. When 8080 interface mode is selected, this pin receives the Read (RD#) signal. Read operation is initiated when this pin is pulled LOW and the chip is selected. When serial or I^2C interface is selected, this pin must be connected to V_{SS}.
D[7:0]	I/O	These pins are bi-directional data bus connecting to the MCU data bus. Unused pins are recommended to tie LOW.

Pin Name	Pin Type	Description
		When serial interface mode is selected, D2, D1 should be tied together as the serial data input: SDIN, and D0 will be the serial clock input: SCLK. When I^2C mode is selected, D2, D1 should be tied together and serve as SDA_{out}, SDA_{in} in application and D0 is the serial clock input, SCL.
MS	I	Connect this pin to V_{LH} to enable the chip for Master chip. Connect this pin to V_{LL} for Slave chip.
D_SEL	I	Reserved pin. It must be connected to V_{LL}.
LS	I	Reserved pin. It must be connected to V_{LL}.
FR	O	This pin outputs RAM write synchronization signal. Proper timing between MCU data writing and frame display timing can be achieved to prevent tearing effect. It should be kept NC if it is not used.
SYNC_MS1	I	Reserved pin. This pin should be kept NC.
IR_MS1	I	Reserved pin. This pin should be kept NC.
IS_MS1	I	Reserved pin. This pin should be kept NC.
CL_MS0	O	Reserved pin. This pin should be kept NC.
SYNC_MS0	O	Reserved pin. This pin should be kept NC.
IR_MS0	O	Reserved pin. This pin should be kept NC.
IS_MS0	O	Reserved pin. This pin should be kept NC.
TR[14:0]	-	Reserved pins. These pins should be kept NC.
VID[1:0]	I	Reserved pin and is recommended to keep it float.
GPIO	I/O	Reserved pin. This pin should be kept NC.
SEG[319:0]	O	These pins provide the OLED segment driving signals. These pins are V_{SS} state when display is OFF.
COM[159:0]	O	These pins provide the Common switch signals to the OLED panel.
NC	-	This is dummy pin. It should be kept NC.

6 FUNCTIONAL BLOCK DESCRIPTIONS

6.1 MCU Interface selection

SSD1363 MCU interface consist of 8 data pins and 5 control pins. The pin assignment at different interface mode is summarized in Table 6-1. Different MCU mode can be set by hardware selection on BS[2:0] pins (please refer to Table 5-2: Bus Interface selection for BS[2:0] setting).

Table 6-1 : MCU interface assignment under different bus interface mode

Pin Name / Bus Interface	Data/Command Interface								Control Signal				
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**E**	**R/W#**	**CS#**	**D/C#**	**RES#**
8-bit 8080	D[7:0]								RD#	WR#	CS#	D/C#	RES#
8-bit 6800	D[7:0]								E	R/W#	CS#	D/C#	RES#
3-wire SPI	Tie LOW					SDIN		SCLK	Tie LOW		CS#	Tie LOW	RES#
4-wire SPI	Tie LOW					SDIN		SCLK	Tie LOW		CS#	D/C#	RES#
I^2C	Tie LOW					SDA_{OUT}	SDA_{IN}	SCL	Tie LOW			SA0	RES#

When serial interface mode is selected, D0 will be the serial clock input: SCLK; D1 and D2 should be tied together as the serial data input: SDIN.

6.1.1 MCU Parallel 6800-series Interface

The parallel interface consists of 8 bi-directional data pins (D[7:0]), R/W#, D/C#, E and CS#.

A LOW in R/W# indicates WRITE operation and HIGH in R/W# indicates READ operation.
A LOW in D/C# indicates COMMAND read/write and HIGH in D/C# indicates DATA read/write.
The E input serves as data latch signal while CS# is LOW. Data is latched at the falling edge of E signal.

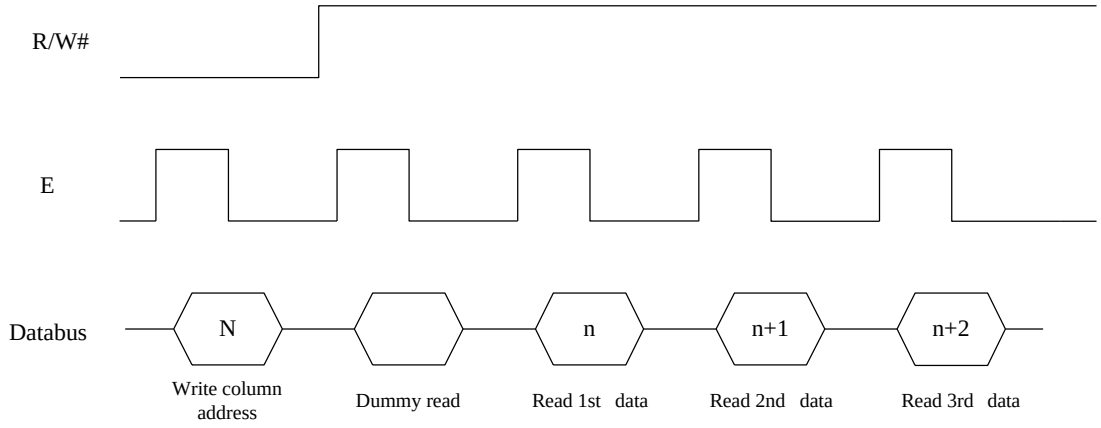
Table 6-2 : Control pins of 6800 interface

Function	E	R/W#	CS#	D/C#
Write command	↓	L	L	L
Read status	↓	H	L	L
Write data	↓	L	L	H
Read data	↓	H	L	H

Note
(1) ↓ stands for falling edge of signal
H stands for HIGH in signal
L stands for LOW in signal

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 6-1.

Figure 6-1 : Data read back procedure - insertion of dummy read



6.1.2 MCU Parallel 8080-series Interface

The parallel interface consists of 8 bi-directional data pins (D[7:0]), RD#, WR#, D/C# and CS#.

A LOW in D/C# indicates COMMAND read/write and HIGH in D/C# indicates DATA read/write.
A rising edge of RD# input serves as a data READ latch signal while CS# is kept LOW.
A rising edge of WR# input serves as a data/command WRITE latch signal while CS# is kept LOW.

Figure 6-2 : Example of Write procedure in 8080 parallel interface mode

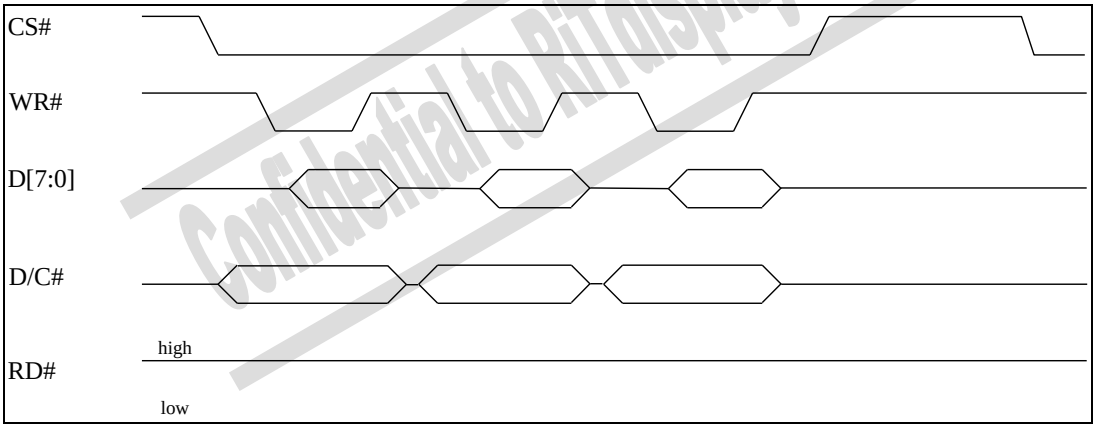


Figure 6-3 : Example of Read procedure in 8080 parallel interface mode

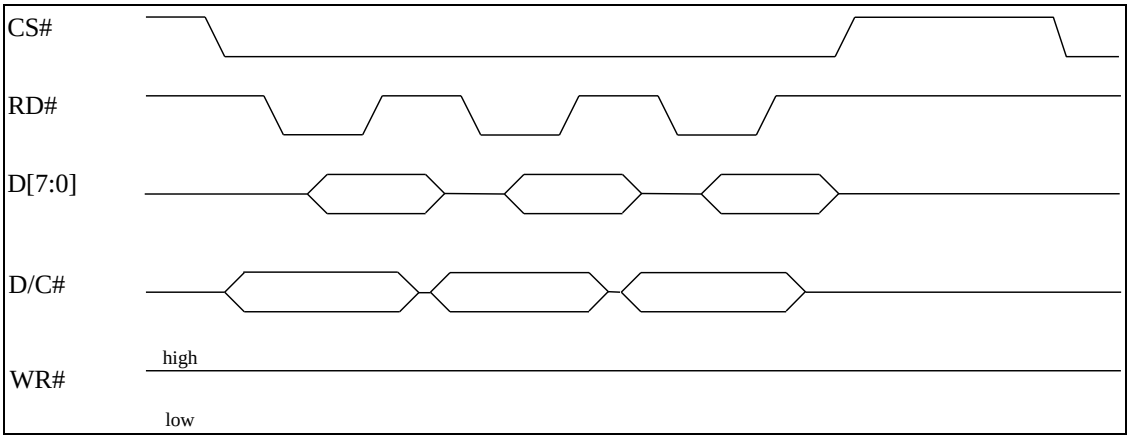


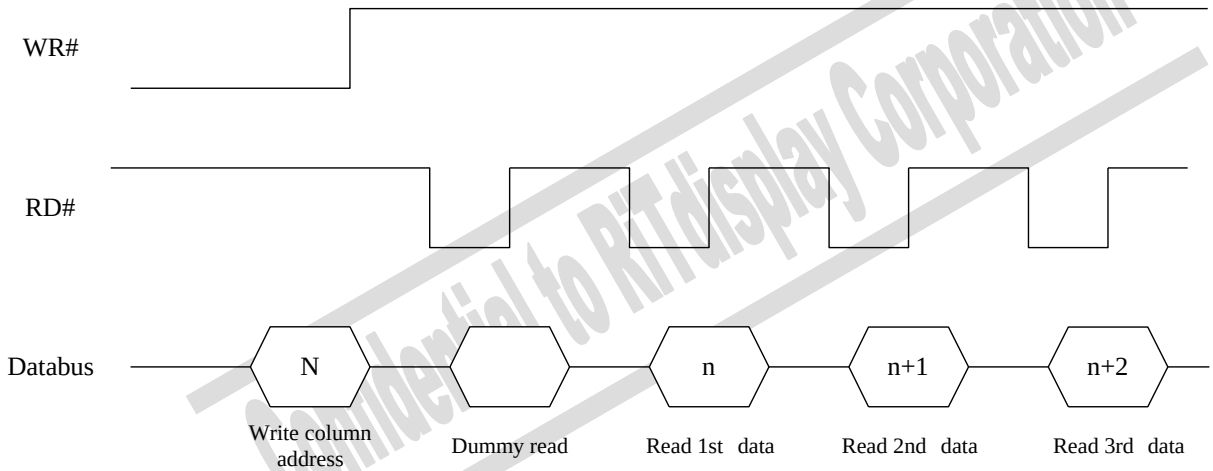
Table 6-3 : Control pins of 8080 interface

Function	RD#	WR#	CS#	D/C#
Write command	H	↑	L	L
Read status	↑	H	L	L
Write data	H	↑	L	H
Read data	↑	H	L	H

Note
(1) ↑ stands for rising edge of signal
(2) H stands for HIGH in signal
(3) L stands for LOW in signal

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 6-4.

Figure 6-4 : Display data read back procedure - insertion of dummy read



6.1.3 MCU Serial Interface (4-wire SPI)

The 4-wire serial interface consists of serial clock: SCLK, serial data: SDIN, D/C#, CS#. In 4-wire SPI mode, D0 acts as SCLK, D1 and D2 are tied together to act as SDIN. For the unused data pins from D3 to D7, E(RD#) and R/W#(WR#) can be connected to an external ground.

Table 6-4 : Control pins of 4-wire Serial interface

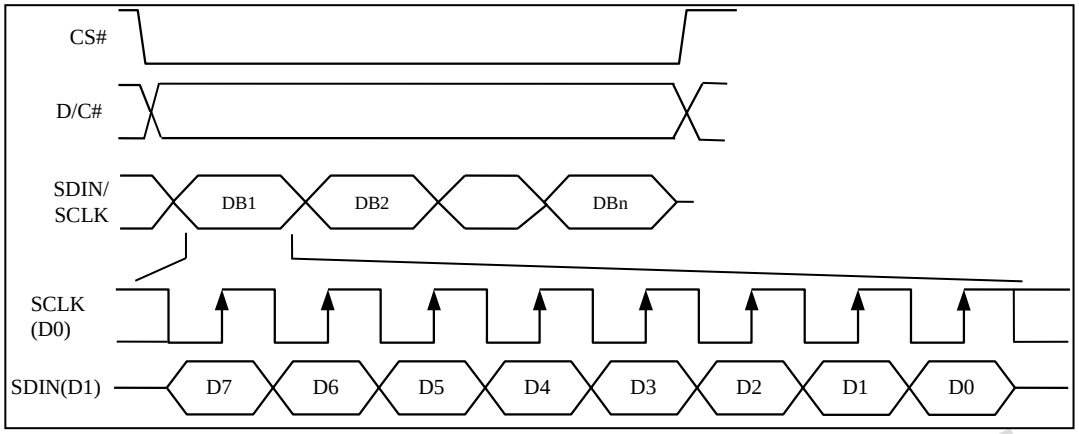
Function	E	R/W#	CS#	D/C#	D0
Write command	Tie LOW	Tie LOW	L	L	↑
Write data	Tie LOW	Tie LOW	L	H	↑

Note
(1) H stands for HIGH in signal
(2) L stands for LOW in signal
(3) ↑ stands for rising edge of signal

SDIN is shifted into an 8-bit shift register on every rising edge of SCLK in the order of D7, D6, ..., D0. D/C# is sampled on every eighth clock and D/C# should be kept stable throughout eight clock period. The data byte in the shift register is written to the Graphic Display Data RAM (GDDRAM) or command register in the same clock.

Under serial mode, only write operations are allowed.

Figure 6-5 : Write procedure in 4-wire Serial interface mode



6.1.4 MCU Serial Interface (3-wire SPI)

The 3-wire serial interface consists of serial clock SCLK, serial data SDIN and CS#.
In 3-wire SPI mode, D0 acts as SCLK, D1 and D2 are tied together to act as SDIN. For the unused data pins from D3 to D7, R/W# (WR#), E(RD#) and D/C# can be connected to an external ground.

The operation is similar to 4-wire serial interface while D/C# pin is not used. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence: D/C# bit, D7 to D0 bit. The D/C# bit (first bit of the sequential data) will determine the following data byte in the shift register is written to the Display Data RAM (D/C# bit = 1) or the command register (D/C# bit = 0).

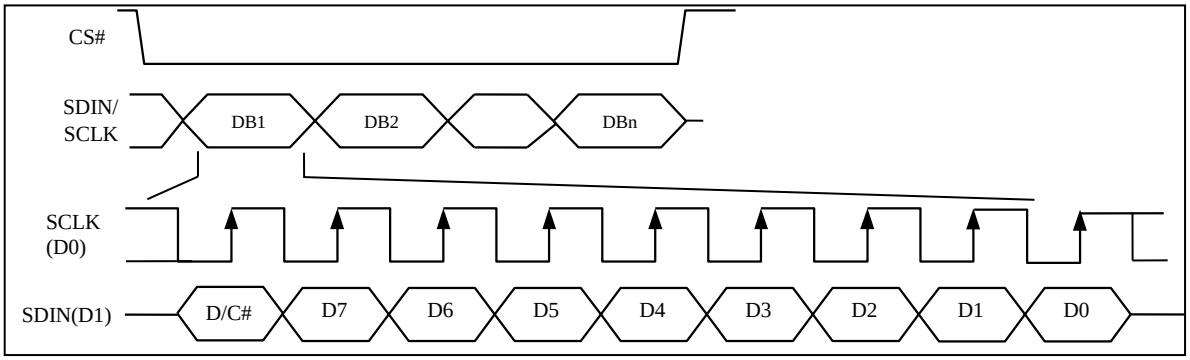
Under serial mode, only write operations are allowed.

Table 6-5 : Control pins of 3-wire Serial interface

Function	E(RD#)	R/W#(WR#)	CS#	D/C#	D0
Write command	Tie LOW	Tie LOW	L	Tie LOW	↑
Write data	Tie LOW	Tie LOW	L	Tie LOW	↑

Note
(1) L stands for LOW in signal
(2) ↑ stands for rising edge of signal

Figure 6-6 : Write procedure in 3-wire Serial interface mode



6.1.5 MCU I²C Interface

The I²C communication interface consists of slave address bit SA0, I²C-bus data signal SDA (SDA_{OUT}/D_2 for output and SDA_{IN}/D_1 for input) and I²C-bus clock signal SCL (D_0). Both the data and clock signals must be connected to pull-up resistors. RES# is used for the initialization of device.

a) Slave address bit (SA0)
SSD1320 has to recognize the slave address before transmitting or receiving any information by the I²C-bus. The device will respond to the slave address following by the slave address bit ("SA0" bit) and the read/write select bit ("R/W#" bit) with the following byte format,

b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
0	1	1	1	1	0	SA0	R/W#

"SA0" bit provides an extension bit for the slave address. Either "0111100" or "0111101", can be selected as the slave address of SSD1320. D/C# pin acts as SA0 for slave address selection. "R/W#" bit is used to determine the operation mode of the I²C-bus interface. R/W#=1, it is in read mode. R/W#=0, it is in write mode.

b) I²C-bus data signal (SDA)
SDA acts as a communication channel between the transmitter and the receiver. The data and the acknowledgement are sent through the SDA.

It should be noticed that the ITO track resistance and the pulled-up resistance at "SDA" pin becomes a voltage potential divider. As a result, the acknowledgement would not be possible to attain a valid logic 0 level in "SDA".

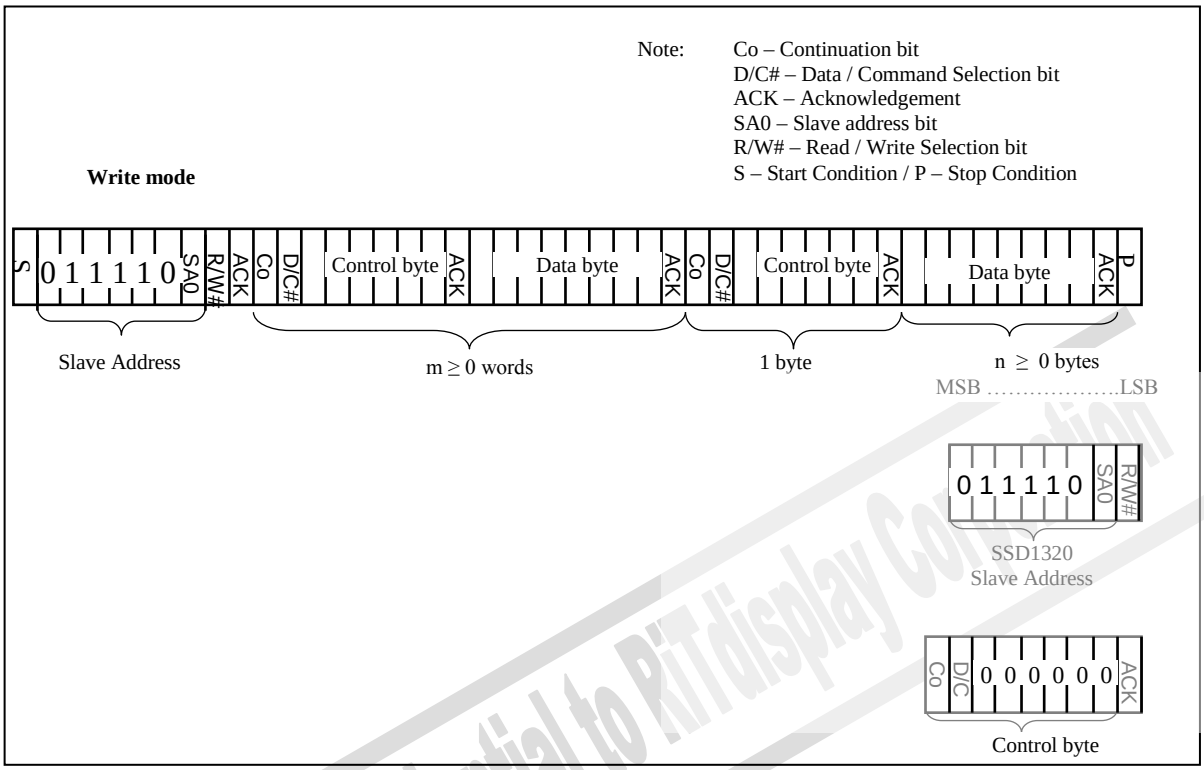
"SDA_{IN}" and "SDA_{OUT}" are tied together and serve as SDA. The "SDA_{IN}" pin must be connected to act as SDA. The "SDA_{OUT}" pin may be disconnected. When "SDA_{OUT}" pin is disconnected, the acknowledgement signal will be ignored in the I²C-bus.

c) I²C-bus clock signal (SCL)
The transmission of information in the I²C-bus is following a clock signal, SCL. Each transmission of data bit is taken place during a single clock period of SCL.

6.1.5.1 I²C-bus Write data

The I²C-bus interface gives access to write data and command into the device. Please refer to Figure 6-7 for the write mode of I²C-bus in chronological order.

Figure 6-7 : I²C-bus data format



6.1.5.2 Write mode for I²C

1) The master device initiates the data communication by a start condition. The definition of the start condition is shown in Figure 6-8. The start condition is established by pulling the SDA from HIGH to LOW while the SCL stays HIGH.
2) The slave address is following the start condition for recognition use. For the SSD1320, the slave address is either "b0111100" or "b0111101" by changing the SA0 to LOW or HIGH (D/C pin acts as SA0).
3) The write mode is established by setting the R/W# bit to logic "0".
4) An acknowledgement signal will be generated after receiving one byte of data, including the slave address and the R/W# bit. Please refer to Figure 6-9 for the graphical representation of the acknowledge signal. The acknowledge bit is defined as the SDA line is pulled down during the HIGH period of the acknowledgement related clock pulse.
5) After the transmission of the slave address, either the control byte or the data byte may be sent across the SDA. A control byte mainly consists of Co and D/C# bits following by six "0" 's.
    a. If the Co bit is set as logic "0", the transmission of the following information will contain data bytes only.
    b. The D/C# bit determines the next data byte is acted as a command or a data. If the D/C# bit is set to logic "0", it defines the following data byte as a command. If the D/C# bit is set to logic "1", it defines the following data byte as a data which will be stored at the GDDRAM. The GDDRAM column address pointer will be increased by one automatically after each data write.
6) Acknowledge bit will be generated after receiving each control byte or data byte.
7) The write mode will be finished when a stop condition is applied. The stop condition is also defined in Figure 6-8. The stop condition is established by pulling the "SDA in" from LOW to HIGH while the "SCL" stays HIGH.

Figure 6-8 : Definition of the Start and Stop Condition

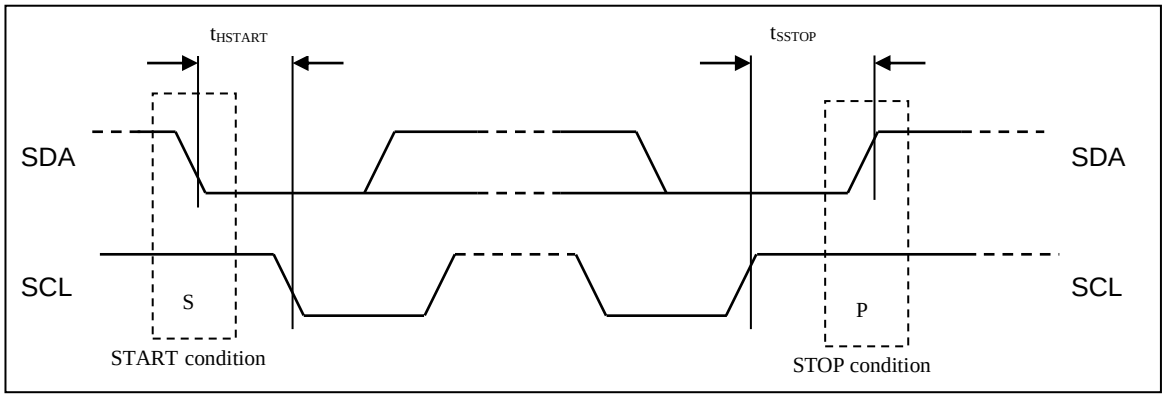
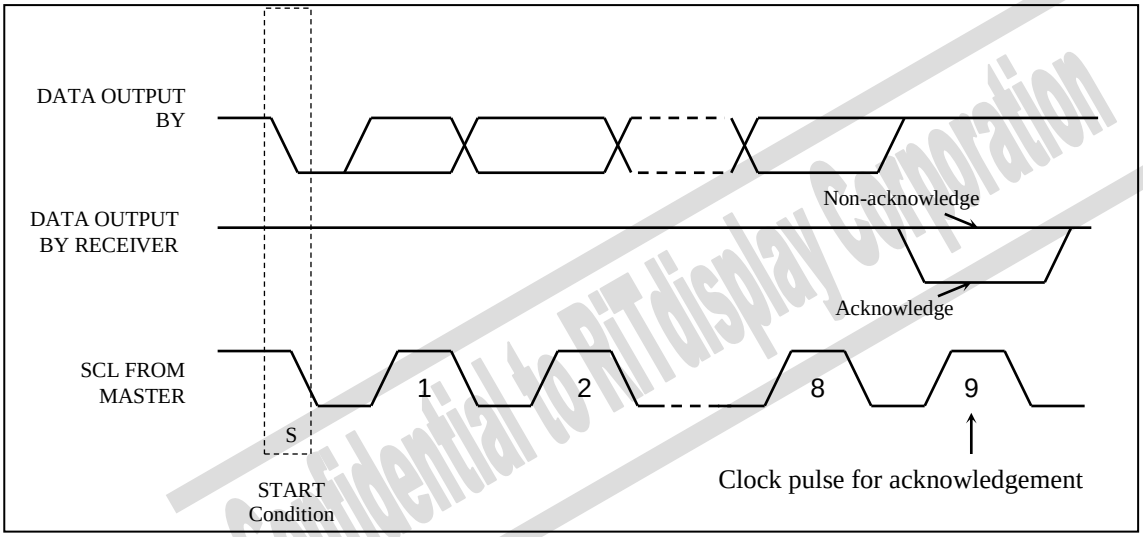


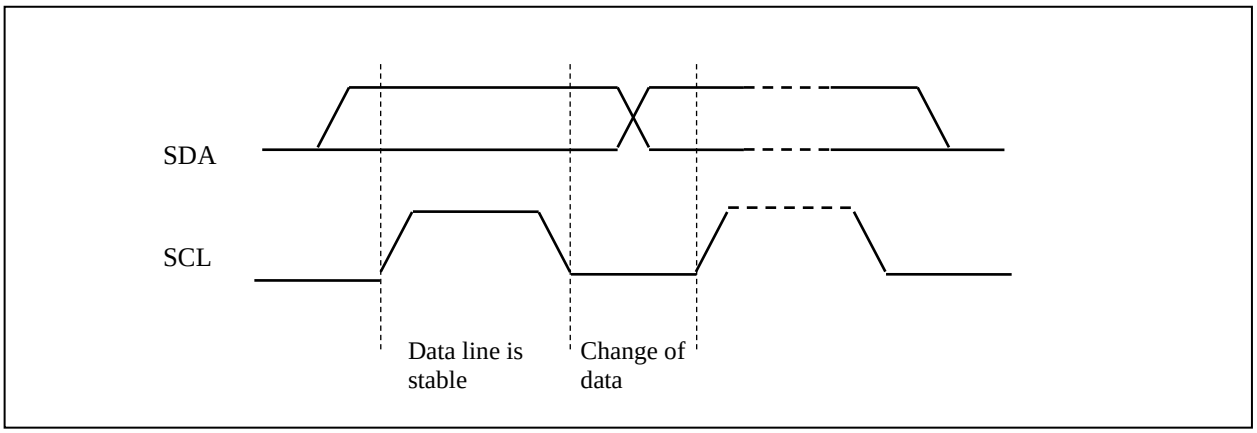
Figure 6-9 : Definition of the acknowledgement condition



Please be noted that the transmission of the data bit has some limitations.

1. The data bit, which is transmitted during each SCL pulse, must keep at a stable state within the "HIGH" period of the clock pulse. Please refer to the
2. Figure 6-10 for graphical representations. Except in start or stop conditions, the data line can be switched only when the SCL is LOW.
3. Both the data line (SDA) and the clock line (SCL) should be pulled up by external resistors.

Figure 6-10 : Definition of the data transfer condition



6.2 GDDRAM

6.2.1 GDDRAM structure in Gray Scale mode

The GDDRAM address map in Table 6-6 shows the GDDRAM in Gray Scale mode. Since in Gray Scale mode, there are 16 gray levels. Therefore four bits (one nibble) are allocated for each pixel. For example D25440[3:0] in Table 6-6 corresponds to the pixel located in (COM159, SEG2). So the lower nibble and higher nibble of D0, D1, D2, …, D25597, D25598, D25599 in Table 6-6 represent the 320x160 data nibbles in the GDDRAM.

Table 6-6 : GDDRAM in Gray Scale mode (RESET)

		SEG0	SEG1	SEG2	SEG3		SEG316	SEG317	SEG31	SEG319	SEG Outputs
		00		00			4F		4F		RAM Column address (HEX)
COM0	00	D1[3:0]	D1[7:4]	D0[3:0]	D0[7:4]		D159[3:0]	D159[7:4]	D158[3:0]	D158[7:4]	
COM1	01	D161[3:0]	D161[7:4]	D160[3:0]	D160[7:4]		D319[3:0]	D319[7:4]	D318[3:0]	D318[7:4]	
|	|									
COM158	9E	D25281[3:0]	D25281[7:4]	D25280[3:0]	D25280[7:4]		D25439[3:0]	D25439[7:4]	D25438[3:0]	D25438[7:4]	
COM159	9F	D25441[3:0]	D25441[7:4]	D25440[3:0]	D25440[7:4]		D25599[3:0]	D25599[7:4]	D25598[3:0]	D25598[7:4]	
COM Outputs	RAM Row Address (HEX)										

Corresponding to one pixel

6.2.2 Data bus to RAM mapping

Table 6-7 : Data bus usage

Read / Write Data		**Data bus D[7:0]**							
Bus width	**Input order**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
8 bits	1st	3	3	3	3	2	2	2	2
	2nd	1	1	1	1	0	0	0	0

Corresponding to one pixel

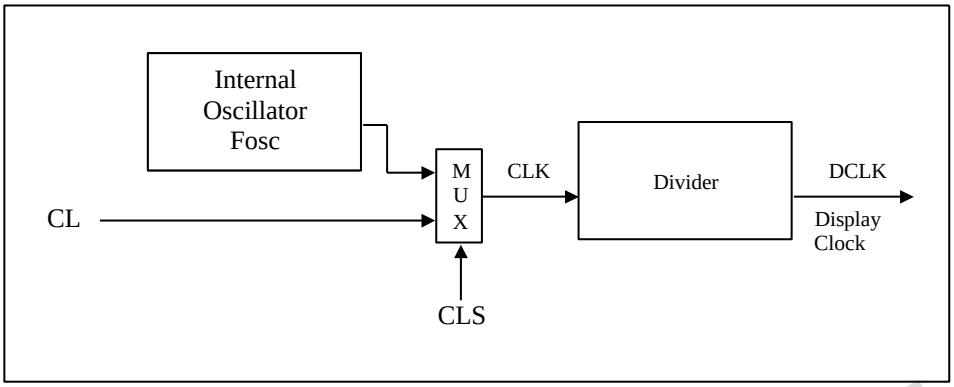
6.3 Command Decoder

This module determines whether the input data is interpreted as data or command. Data is interpreted based upon the input of the D/C# pin.

If D/C# pin is HIGH, D[7:0] is interpreted as display data written to Graphic Display Data RAM (GDDRAM). If it is LOW, the input at D[7:0] is interpreted as a command. Then data input will be decoded and written to the corresponding command register.

6.4 Oscillator Circuit and Display Time Generator

Figure 6-11 : Oscillator Circuit and Display Time Generator



This module is an on-chip LOW power RC oscillator circuitry. The operation clock (CLK) can be generated either from internal oscillator or external source CL pin. This selection is done by CLS pin. If CLS pin is pulled HIGH, internal oscillator is chosen and CL should be connected to V_{LL}. Pulling CLS pin LOW disables internal oscillator and external clock must be connected to CL pins for proper operation. When the internal oscillator is selected, its output frequency Fosc can be changed by command B3h A[7:4].

The display clock (DCLK) for the Display Timing Generator is derived from CLK. The divide ratio "D" can be programmed from 1 to 256 by command B3h

$$DCLK = F_{OSC} / D$$

The frame frequency of display is determined by the following formula.

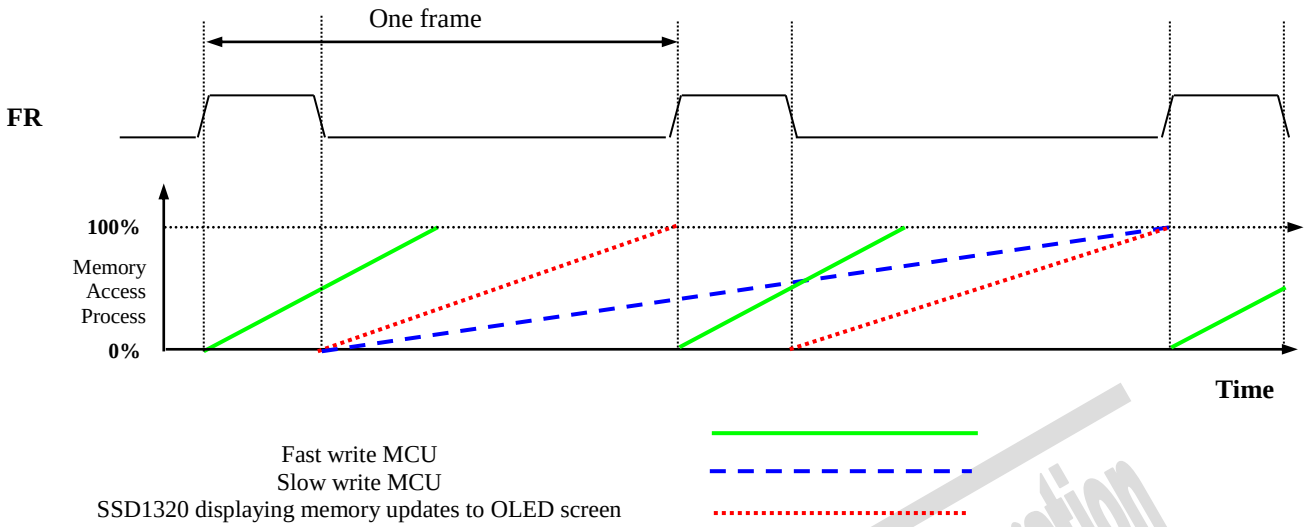
$$F_{FRM} = \frac{F_{osc}}{D \times K \times No.\,of\ Mux}$$

where

- D stands for clock divide ratio. It is set by command B3h A[3:0]. The divide ratio has the range from 1 to 16.
- K is the number of display clocks per row. The value is derived by
  K = Phase 1 period + Phase 2 period + K_o
  K_o = DCLKs in current drive period = 72.
  Default K is 4 + 7 + 72 = 83 at power on reset.
  Please refer to Section 6.8 "SEG / COM Drivers" for the details of the "Phase".
- Number of multiplex ratio is set by command CAh. The power on reset value is 159 (i.e. 160MUX).
- F_{OSC} is the oscillator frequency. It can be changed by command B3h A[7:4]. The higher the register setting results in higher frequency.

6.5 FR synchronization

FR synchronization signal can be used to prevent tearing effect.



The starting time to write a new image to OLED driver is depended on the MCU writing speed. If MCU can finish writing a frame image within one frame period, it is classified as fast write MCU. For MCU needs longer writing time to complete (more than one frame but within two frames), it is a slow write one.

For fast write MCU: MCU should start to write new frame of ram data just after rising edge of FR pulse and should be finished well before the rising edge of the next FR pulse.

For slow write MCU: MCU should start to write new frame ram data after the falling edge of the 1st FR pulse and must be finished before the rising edge of the 3rd FR pulse.

6.6 Reset Circuit

When RES# input is LOW, the chip is initialized with the following status:

1. Display is OFF
2. 160 MUX Display Mode
3. Normal segment and display data column address and row address mapping (SEG0 mapped to address 00h and COM0 mapped to address 00h)
4. Shift register data clear in serial interface
5. Display start line is set at display RAM address 0
6. Column address counter is set at 0
7. Normal scan direction of the COM outputs
8. Contrast control register is set at 7Fh
9. Default linear LUT (Equivalent to B9h command)
10. Normal display mode (Equivalent to A6h command)

6.7 SEG/COM Driving block

This block is used to derive the incoming power sources into the different levels of internal use voltage and current.

- V_{CC} is the most positive voltage supply.
- V_{COMH} is the Common deselected level. It is internally regulated.
- V_{LSS} is the ground path of the analog and panel current.
- I_{REF} is a reference current source for segment current drivers I_{SEG}. The relationship between reference current and segment current is:

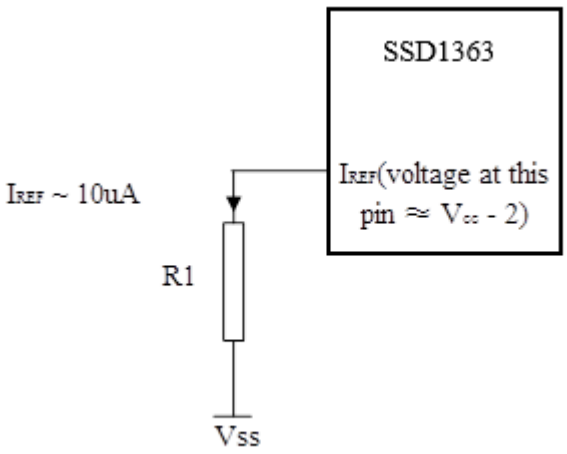
  I_{SEG} = Contrast / 256 x I_{REF} x 48

  in which the contrast (1~255) is set by Set Contrast command C1h

When external I_{REF} is used, the magnitude of I_{REF} is controlled by the value of resistor, which is connected between I_{REF} pin and V_{SS} as shown in Figure 6-12. It is recommended to set I_{REF} to 10 ± 2uA so as to achieve I_{SEG} = 480uA at maximum contrast 255.

SSD1363

Figure 6-12 : I_{REF} Current Setting by Resistor Value



Since the voltage at I_{REF} pin is V_{CC} – 2V, the value of resistor R1 can be found as below:

For I_{REF} = 10uA, V_{CC} =12V:

R1 = (Voltage at I_{REF} – V_{SS}) / I_{REF}
≈ (12 – 2) / 10uA
= 1MΩ

6.8 SEG / COM Drivers

Segment drivers consist of 480 current sources to drive OLED panel. The driving current can be adjusted by altering the registers of the contrast setting command (C1h). Common drivers generate scanning voltage pulse. The block diagrams and waveforms of the segment and common driver are shown as follow.

Figure 6-13 : Segment and Common Driver Block Diagram – Single COM mode

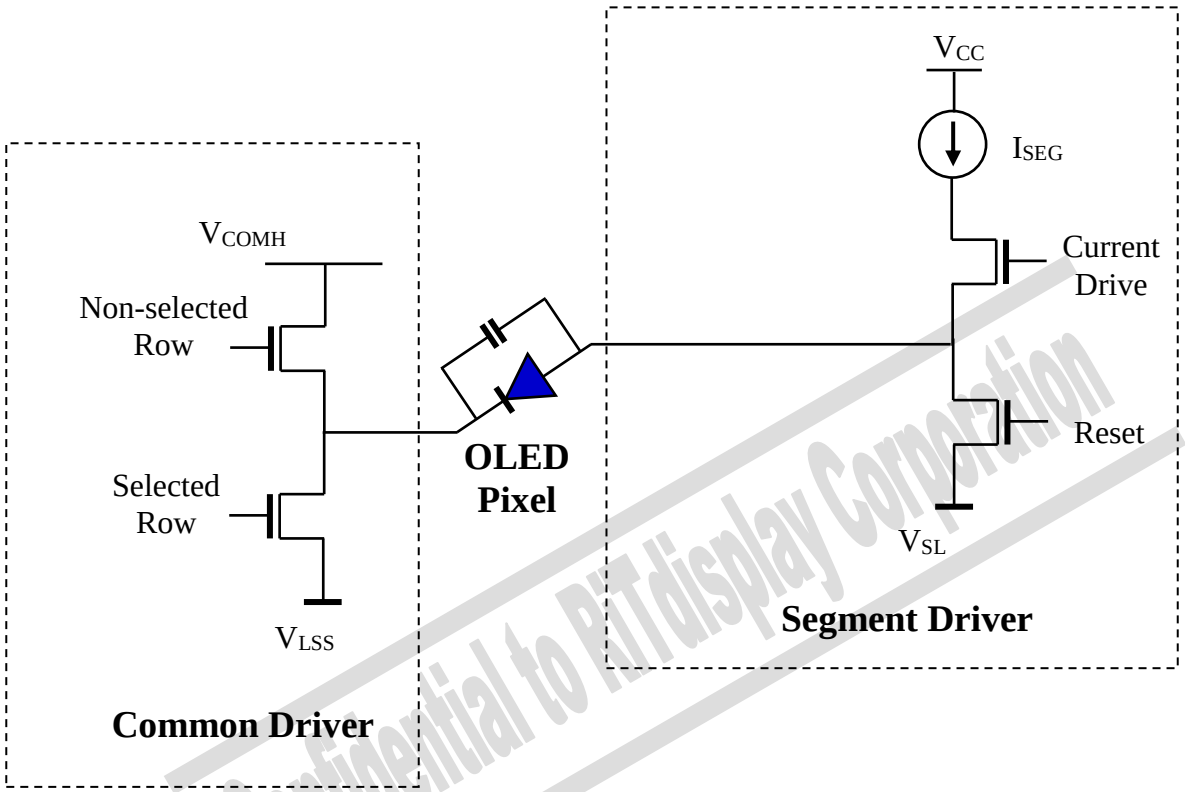
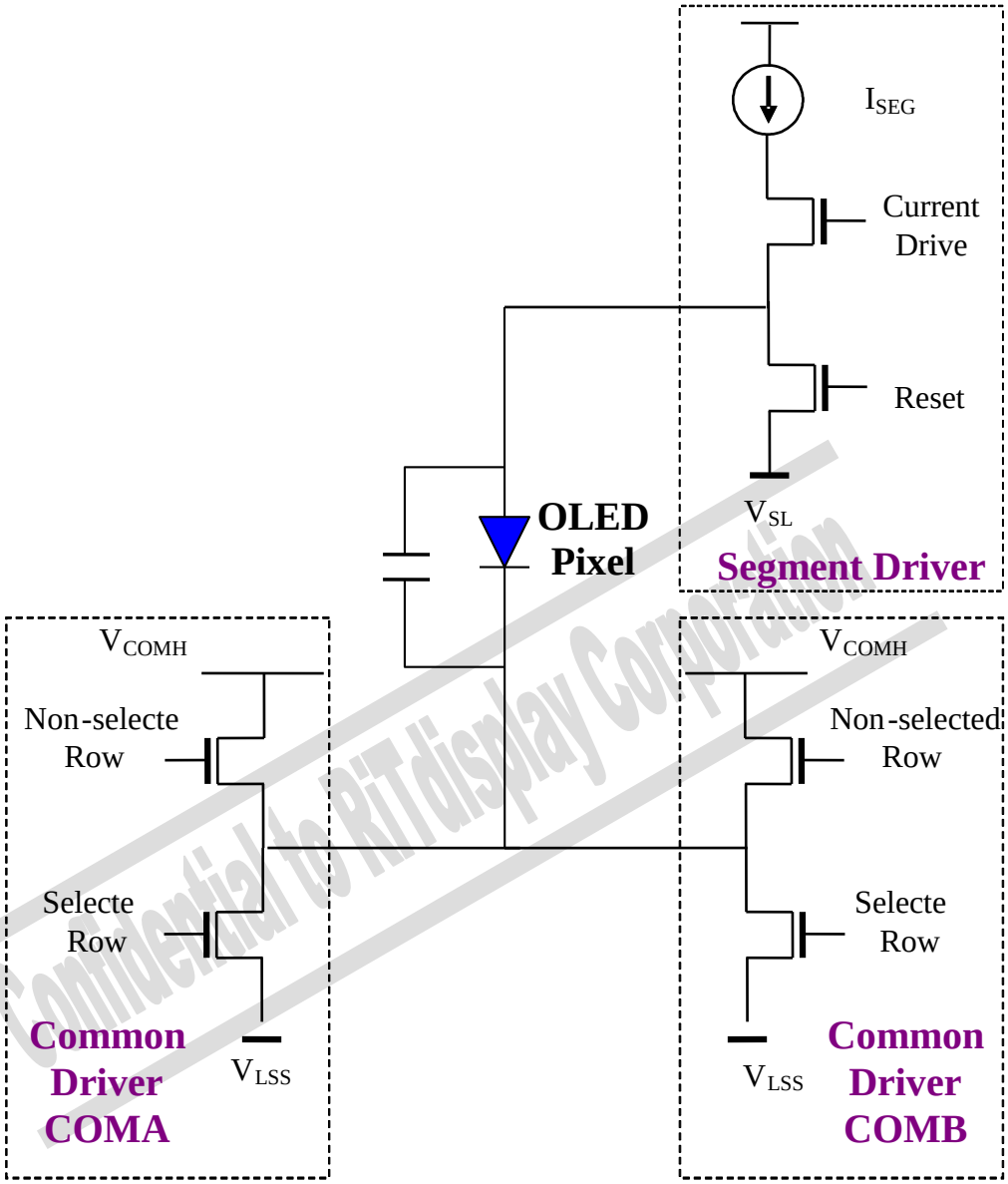


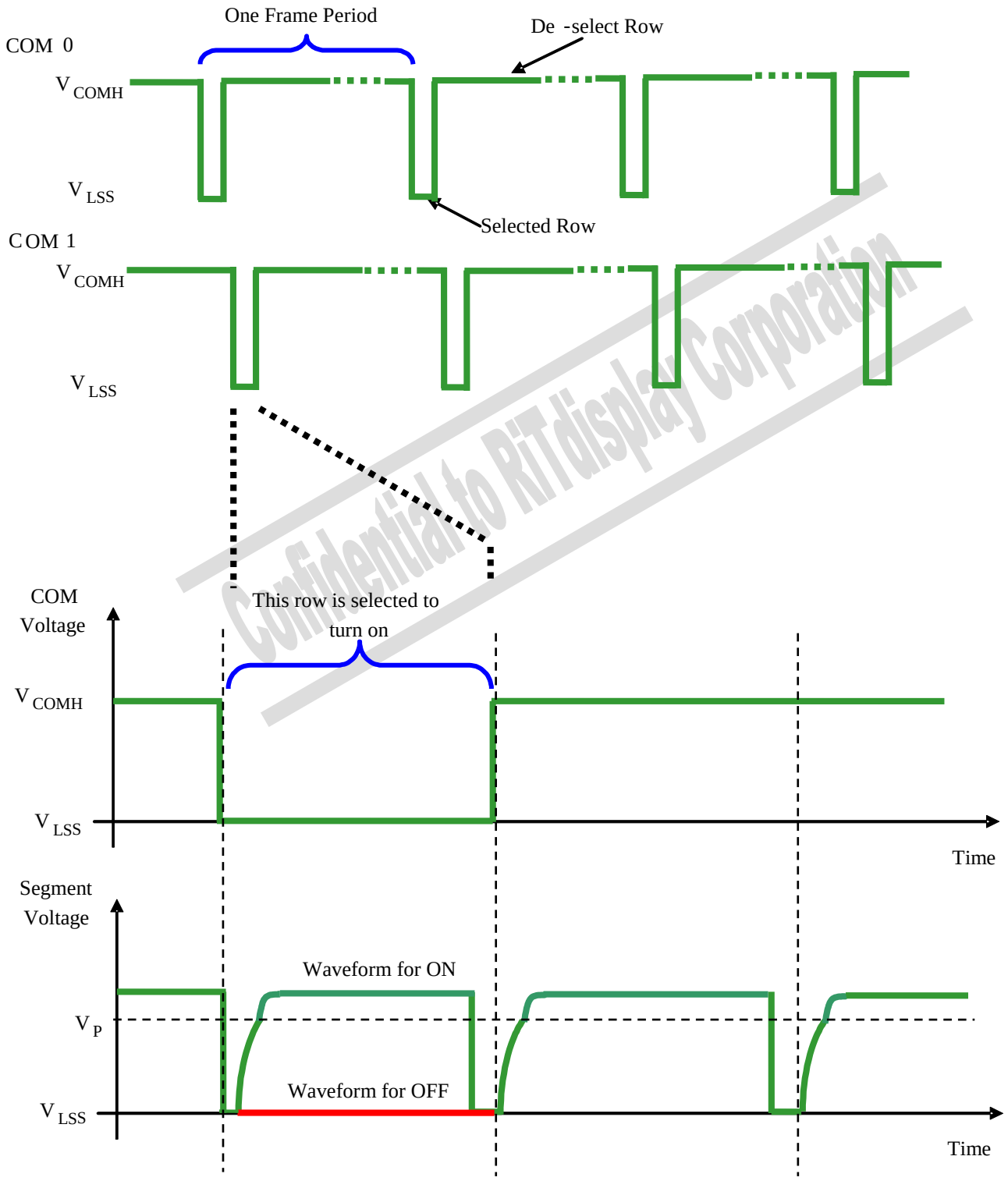
Figure 6-14 : Segment and Common Driver Block Diagram – Dual COM mode



The commons are scanned sequentially, row by row. If a row is not selected, all the pixels on the row are in reverse bias by driving those commons to voltage V_{COMH} as shown in Figure 6-15.

In the scanned row, the pixels on the row will be turned ON or OFF by sending the corresponding data signal to the segment pins. If the pixel is turned OFF, the segment current is disabled and the Reset switch is enabled. On the other hand, the segment drives to I_{SEG} when the pixel is turned ON.

Figure 6-15 : Segment and Common Driver Signal Waveform



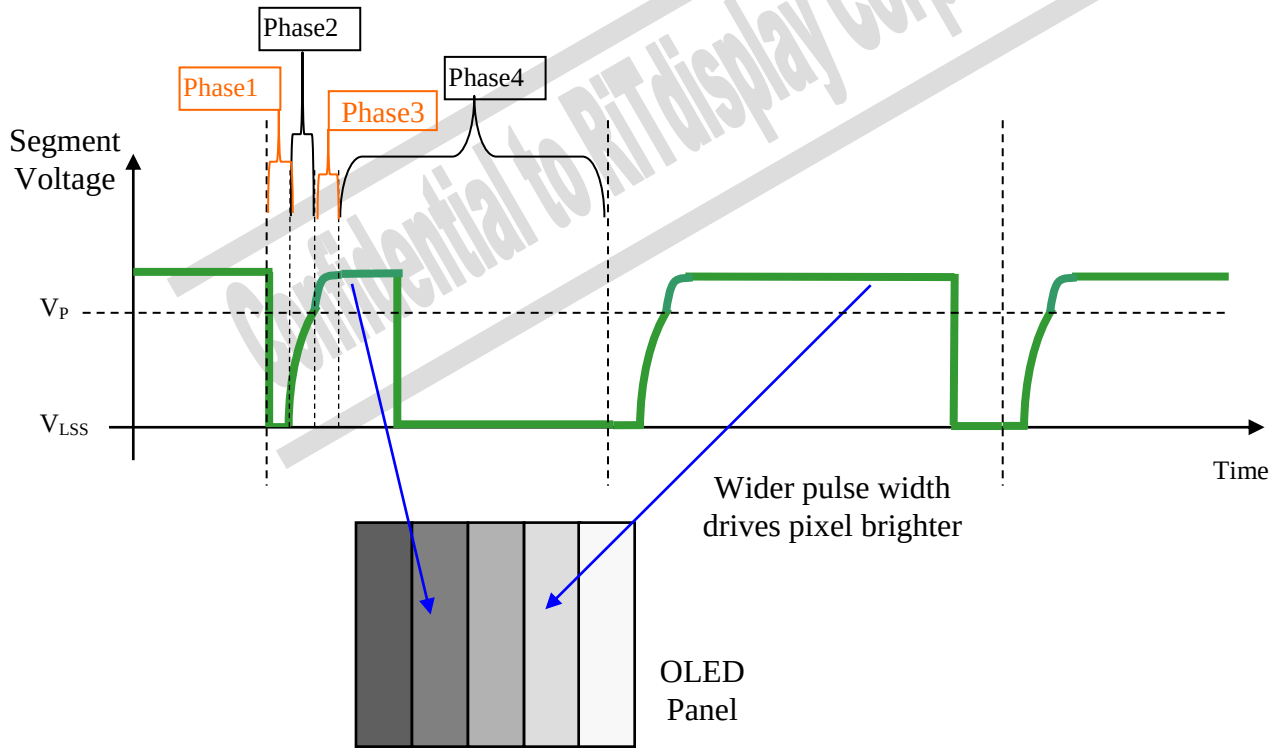
There are four phases to driving an OLED a pixel. In phase 1, the pixel is reset by the segment driver to V_{LSS} in order to discharge the previous data charge stored in the parasitic capacitance along the segment electrode. The period of phase 1 can be programmed by command B1h A[3:0]. An OLED panel with larger capacitance requires a longer period for discharging.

In phase 2, first pre-charge is performed. The pixel is driven to attain the corresponding voltage level V_P from V_{LSS}. The amplitude of V_P can be programmed by the command BBh. The period of phase 2 can be programmed by command B1h A[7:4]. If the capacitance value of the pixel of OLED panel is larger, a longer period is required to charge up the capacitor to reach the desired voltage.

In phase 3, the OLED pixel is driven to the targeted driving voltage through second pre-charge. The second pre-charge can control the speed of the charging process. The period of phase 3 can be programmed by command B6h.

Last phase (phase 4) is current drive stage. The current source in the segment driver delivers constant current to the pixel. The driver IC employs PWM (Pulse Width Modulation) method to control the gray scale of each pixel individually. The gray scale can be programmed into different Gamma settings by command B8h / B9h. The bigger gamma setting in the current drive stage results in brighter pixels and vice versa (Details refer to Section 6.9). This is shown in the following figure.

Figure 6-16 : Gray Scale Control in Segment



After finishing phase 4, the driver IC will go back to phase 1 to display the next row image data. This four-step cycle is run continuously to refresh image display on OLED panel.

The length of phase 4 is defined by command B8h / B9h. In the table, the gray scale is defined in incremental way, with reference to the length of previous table entry.

6.9 Gray Scale Decoder

The gray scale effect is generated by controlling the pulse width (PW) of current drive phase, except GS0 there is no pre-charge (phase 2, 3) and current drive (phase 4). The driving period is controlled by the gray scale settings (setting 0 ~ setting 63). The larger the setting, the wider the pulse width, and the brighter the pixel will be. The Gray Scale Table stores the corresponding gray scale setting of the 16 gray scale levels (GS0~GS15) through the software commands B8h or B9h.

As shown in Figure 6-17, GDDRAM data has 4 bits, represent the 16 gray scale levels from GS0 to GS15. Note that the frame frequency is affected by GS15 setting.

Figure 6-17 : Relation between GDDRAM content and gray scale table entry

GDDRAM data (4 bits)	Gray Scale Table	Default Gamma Setting (Command B9h)
0000	GS0	Setting 0
0001	GS1	Setting 4
0010	GS2	Setting 8
0011	GS3	Setting 12
:	:	:
:	:	:
1101	GS13	Setting 52
1110	GS14	Setting 56
1111	GS15	Setting 60

GS1 has only pre-charge but no current drive stage. The duration of different GS are programmable by command B8h and the maximum pulse width setting is 63 DCLKs.

When setting the Gray Scale Table (by B8h command), the rule below must be followed:
The gray scale is defined in incremental way, with reference to the length of previous table entry:

Setting of GS1 has to be ≥ 0
Setting of GS2 has to be > Setting of GS1
Setting of GS3 has to be > Setting of GS2
:
Setting of GS63 has to be > Setting of GS62

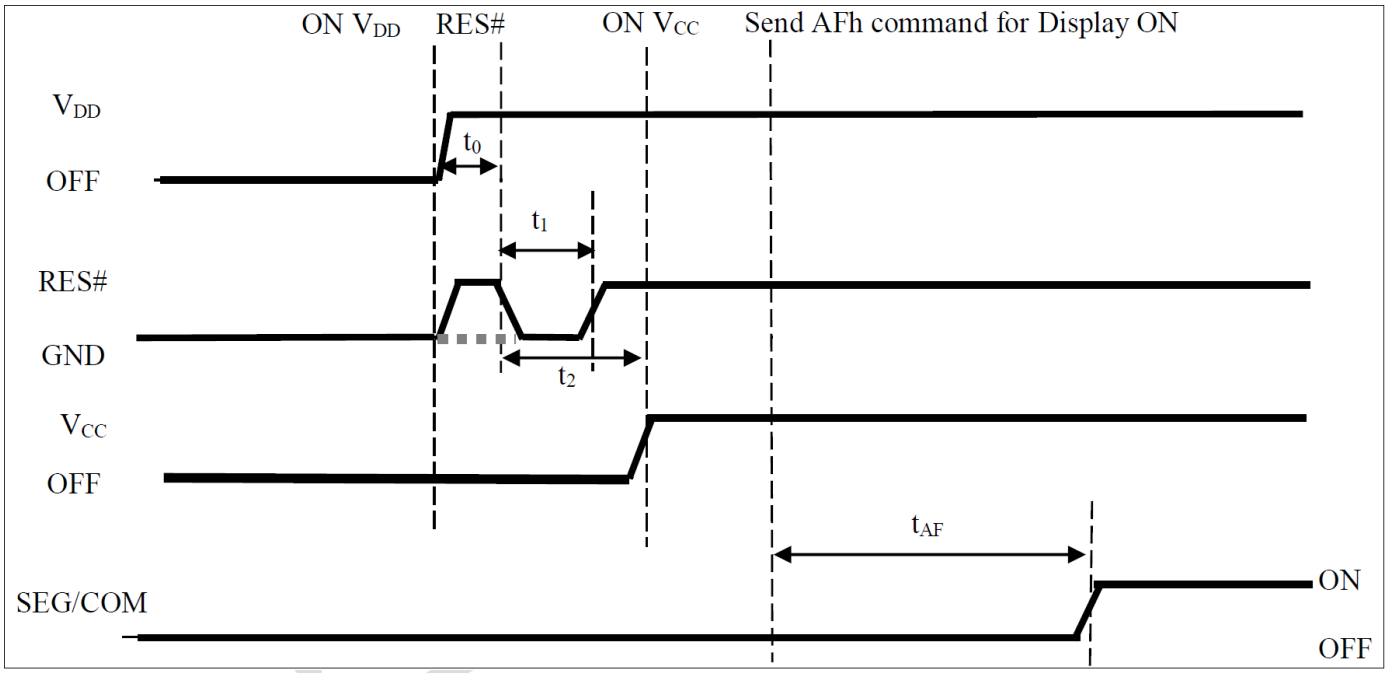
6.10 Power ON and OFF sequence

The following figures illustrate the recommended power ON and power OFF sequence of SSD1363.

Power ON sequence:

1. Power ON V_{DD}
2. After V_{DD} become stable, wait at least 20ms (t_0), set RES# pin LOW (logic low) for at least 3us (t_1) [4] and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 3us (t_2). Then Power ON V_{CC}.[1]
4. After V_{CC} become stable, send command AFh for display ON. SEG/COM will be ON after 100ms (t_{AF}).

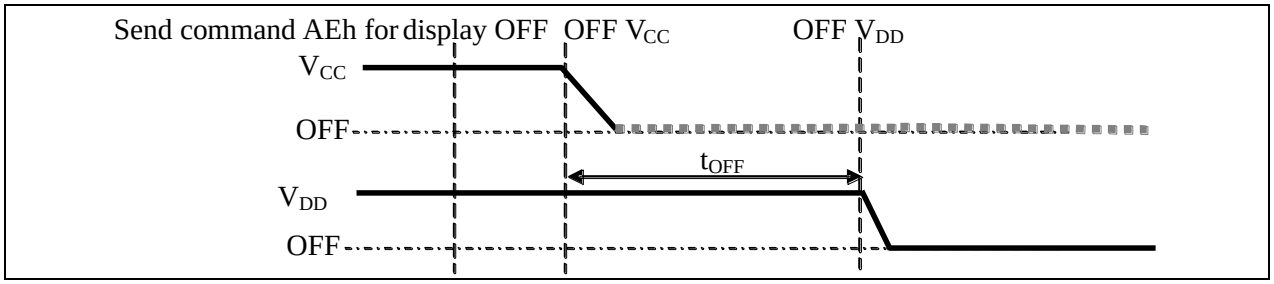
Figure 6-18 : The Power ON sequence



Power OFF sequence:

1. Send command AEh for display OFF.
2. Power OFF V_{CC}.[1], [2]
3. Power OFF V_{DD} after t_{OFF}. [4] (where Minimum t_{OFF}=0ms, typical t_{OFF}=100ms)

Figure 6-19 : The Power OFF sequence



Note:

[1] V_{CC} should be kept float (i.e. disable) when it is OFF.
[2] Power Pins (V_{DD}, V_{CC}) can never be pulled to ground under any circumstance.
[3] The register values are reset after t_1.
[4] V_{DD} should not be Power OFF before V_{CC} Power OFF.

7 MAXIMUM RATINGS

Table 7-1 : Maximum Ratings

(Voltage Reference to V_{SS})

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to 19.0	V
V_{DD}		-0.3 to 4.0	V
V_{SEG}	SEG output voltage	0 to V_{CC}	V
V_{COM}	COM output voltage	0 to 0.9*V_{CC}	V
V_{in}	Input voltage	Vss-0.3 to V_{DD}+0.3	V
T_A	Operating Temperature	-40 to +85	ºC
T_{stg}	Storage Temperature Range	-65 to +150	ºC

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description.

*This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

8 DC CHARACTERISTICS

Conditions (Unless otherwise specified):

Voltage referenced to V_{SS}

V_{DD} = 1.65 to 3.5V

T_A = 25°C

Table 8-1 : DC Characteristics

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{CC}	Operating Voltage	-	8	-	18	V
V_{DD}	Low voltage power supply, power Supply for I/O pins	-	1.65	-	3.5	V
V_{OH}	High Logic Output Level	Iout = 100uA	0.9*V_{DD}	-	V_{DD}	V
V_{OL}	Low Logic Output Level	Iout = 100uA	0	-	0.1*V_{DD}	V
V_{IH}	High Logic Input Level	-	0.8*V_{DD}	-	V_{DD}	V
V_{IL}	Low Logic Input Level	-	0	-	0.2*V_{DD}	V
I_{SLP_VDD}	V_{DD} Sleep mode Current	V_{DD} = 1.65V~3.5V, V_{CC} = 8V~18V, Display OFF, No panel attached	-	-	10	uA
I_{SLP_VCC}	V_{CC} Sleep mode Current	V_{DD} = 1.65V~3.5V, V_{CC} = 8V~18V, Display OFF, No panel attached	-	-	10	uA
I_{DD}	V_{DD} Supply Current	V_{DD} = 2.8V, V_{CC} = 15V, Display ON, No panel attached, contrast = FFh	-	850	-	uA
I_{CC}	V_{CC} Supply Current	V_{DD} = 2.8V, V_{CC} = 15V, Display ON, No panel attached, contrast = FFh	-	1.9	-	mA
I_{SEG}	Segment Output Current Setting V_{CC}=18V, I_{REF}=10uA	Contrast = FF	-	480	-	uA
		Contrast = 7F	-	240	-	uA
		Contrast = 3F	-	120	-	uA
Dev	Segment output current uniformity	Dev = (I_{SEG} – I_{MID}) / I_{MID} I_{MID} = (I_{MAX} + I_{MIN}) / 2 I_{SEG} = Segment current at contrast FF	-3	-	3	%
Adj. Dev	Adjacent pin output current uniformity (contrast setting = FFh)	Adj Dev = (I[n]-I[n+1]) / (I[n]+I[n+1])	-2	-	2	%

9 AC CHARACTERISTICS

Conditions (Unless otherwise specified):

Voltage referenced to V_{SS}

T_A = 25°C

Table 9-1 : AC Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
F_{OSC} (1)	Oscillation Frequency of Display Timing Generator	V_{DD} =2.8V	1.19	1.33	1.47	MHz
F_{FRM}	Frame Frequency for 160 MUX Mode	320x160 Graphic Display Mode, Display ON, Internal Oscillator Enabled	-	F_{OSC} * 1/(D*K*160) (2)	-	Hz
t_{RES}	Reset low pulse width (RES#)	-	3	-	-	us

Note

(1) F_{OSC} stands for the frequency value of the internal oscillator and the value is measured when command B3h A[7:4] is in default value, and B3h A[3:0] is in [0000].

(2) D: divide ratio set by command B3h A[3:0]
K: Phase 1 period + Phase 2 period + X
X: DCLKs in current drive period

Table 9-2 : 6800-Series MCU Parallel Interface Timing Characteristics

(V_{DD}- V_{SS} =1.65V to 3.5V, T_A = 25℃)

Symbol	Parameter	Min	Typ	Max	Unit
t_{CYCLE}	Clock Cycle Time (write)	300	-	-	ns
t_{AS}	Address Setup Time	5	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Figure 9-1 : 6800-series MCU parallel interface characteristics

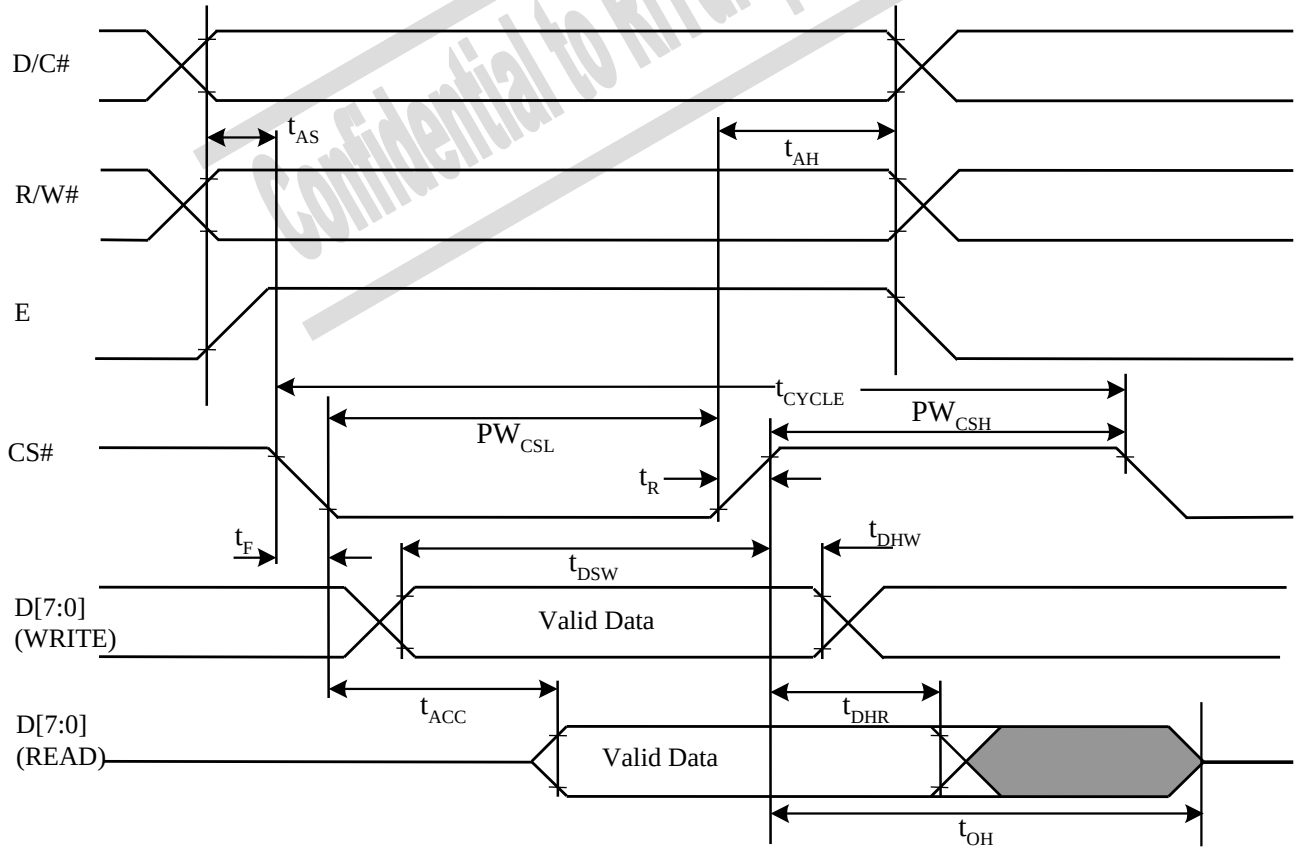


Table 9-3 : 8080-Series MCU Parallel Interface Timing Characteristics

(V_{DD}- V_{SS} =1.65V to 3.5V, T_A = 25℃)

Symbol	Parameter	Min	Typ	Max	Unit
t_{CYCLE}	Clock Cycle Time (write)	300	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	30	-	-	ns
t_{DHW}	Write Data Hold Time	20	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
t_{PWLR}	Read Low Time	120	-	-	ns
t_{PWLW}	Write Low Time	60	-	-	ns
t_{PWHR}	Read High Time	60	-	-	ns
t_{PWHW}	Write High Time	60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns
t_{CS}	Chip select setup time	0	-	-	ns
t_{CSH}	Chip select hold time to read signal	0	-	-	ns
t_{CSF}	Chip select hold time	20	-	-	ns

Figure 9-2 : 8080-series MCU parallel interface characteristics

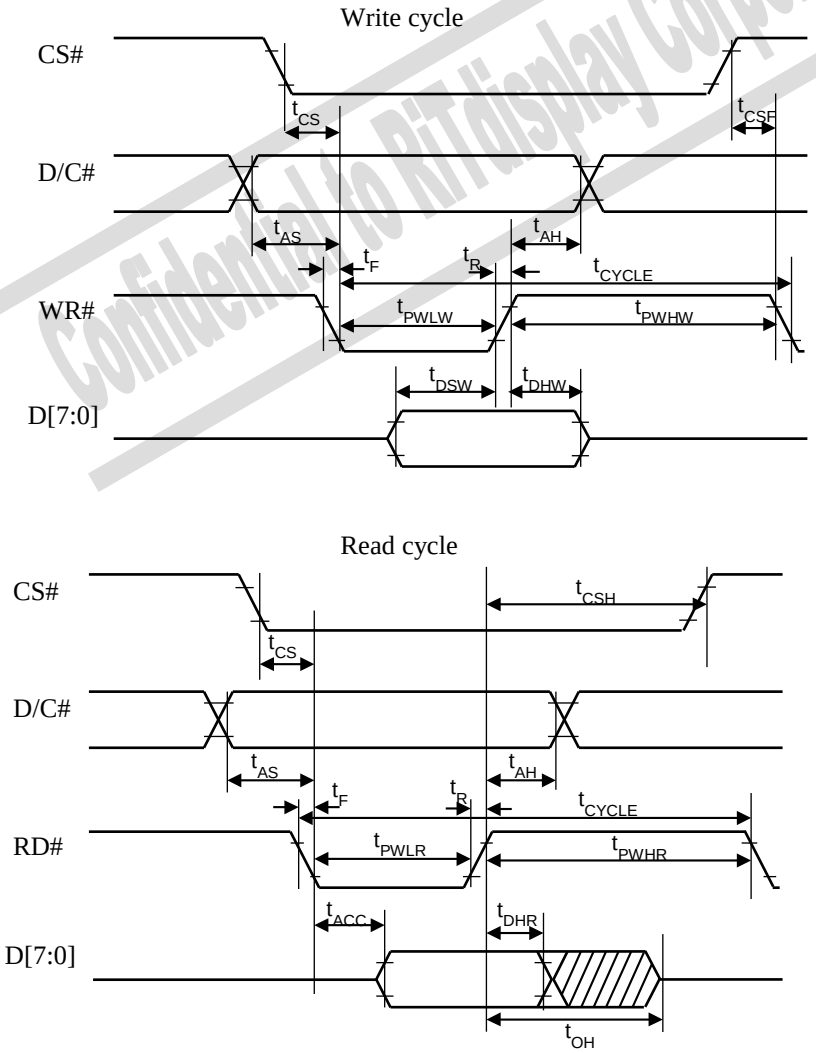


Table 9-4 : Serial Interface Timing Characteristics (4-wire SPI)

(V_{DD}- V_{SS} =1.65V to 3.5V, T_A = 25℃)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	50	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	10	-	-	ns
t_{CSS}	Chip Select Setup Time	10	-	-	ns
t_{CSH}	Chip Select Hold Time	10	-	-	ns
t_{DSW}	Write Data Setup Time	10	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{CLKL}	Clock Low Time	15	-	-	ns
t_{CLKH}	Clock High Time	20	-	-	ns
t_R	Rise Time	-	-	10	ns
t_F	Fall Time	-	-	10	ns

Figure 9-3 : Serial interface characteristics (4-wire SPI)

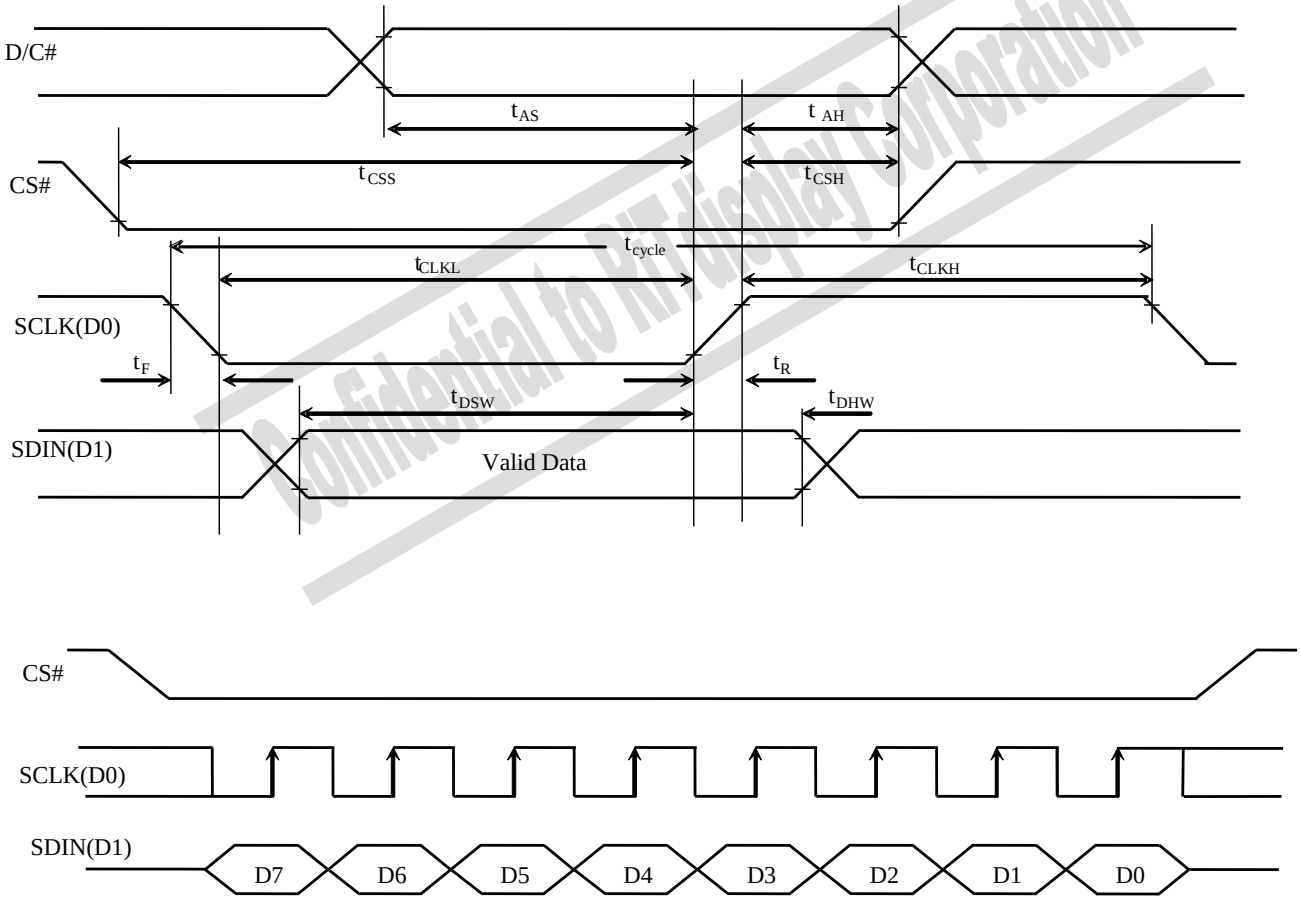


Table 9-5 : Serial Interface Timing Characteristics (3-wire SPI)

(V_{DD}- V_{SS} =1.65V to 3.5V, T_A = 25℃)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	50	-	-	ns
t_{CSS}	Chip Select Setup Time	10	-	-	ns
t_{CSH}	Chip Select Hold Time	10	-	-	ns
t_{DSW}	Write Data Setup Time	10	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{CLKL}	Clock Low Time	15	-	-	ns
t_{CLKH}	Clock High Time	20	-	-	ns
t_R	Rise Time	-	-	10	ns
t_F	Fall Time	-	-	10	ns

Figure 9-4 : Serial interface characteristics (3-wire SPI)

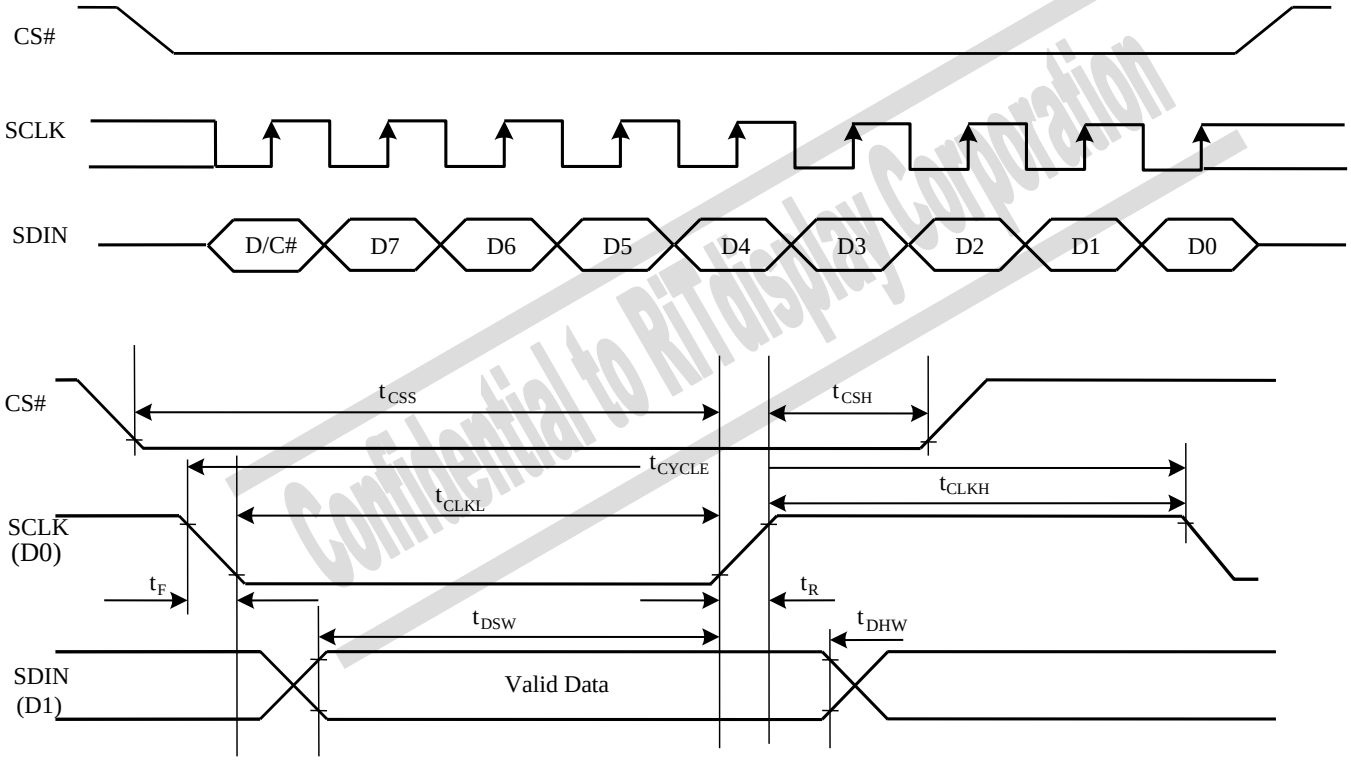
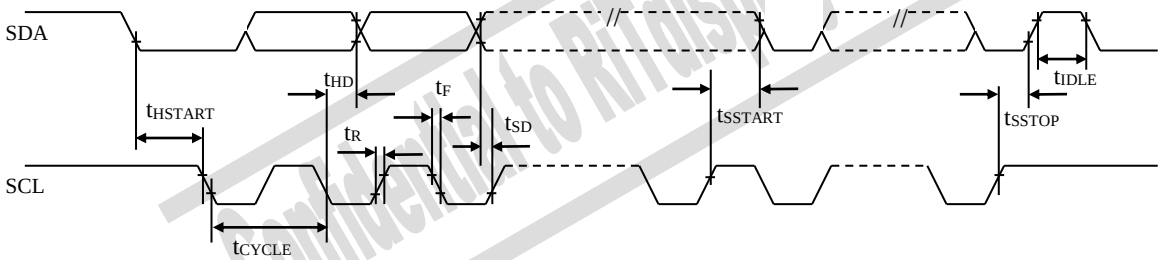


Table 9-6 : I²C Interface Timing Characteristics

(V_{DD}- V_{SS} =1.65V to 3.5V, T_A = 25℃)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	2.5	-	-	us
t_{HSTART}	Start condition Hold Time	0.6	-	-	us
t_{HD}	Data Hold Time (for "SDA_{OUT}" pin)	0	-	-	ns
	Data Hold Time (for "SDA_{IN}" pin)	300	-	-	ns
t_{SD}	Data Setup Time	100	-	-	ns
t_{SSTART}	Start condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	-	us
t_{SSTOP}	Stop condition Setup Time	0.6	-	-	us
t_R	Rise Time for data and clock pin	-	-	300	ns
t_F	Fall Time for data and clock pin	-	-	300	ns
t_{IDLE}	Idle Time before a new transmission can start	1.3	-	-	us

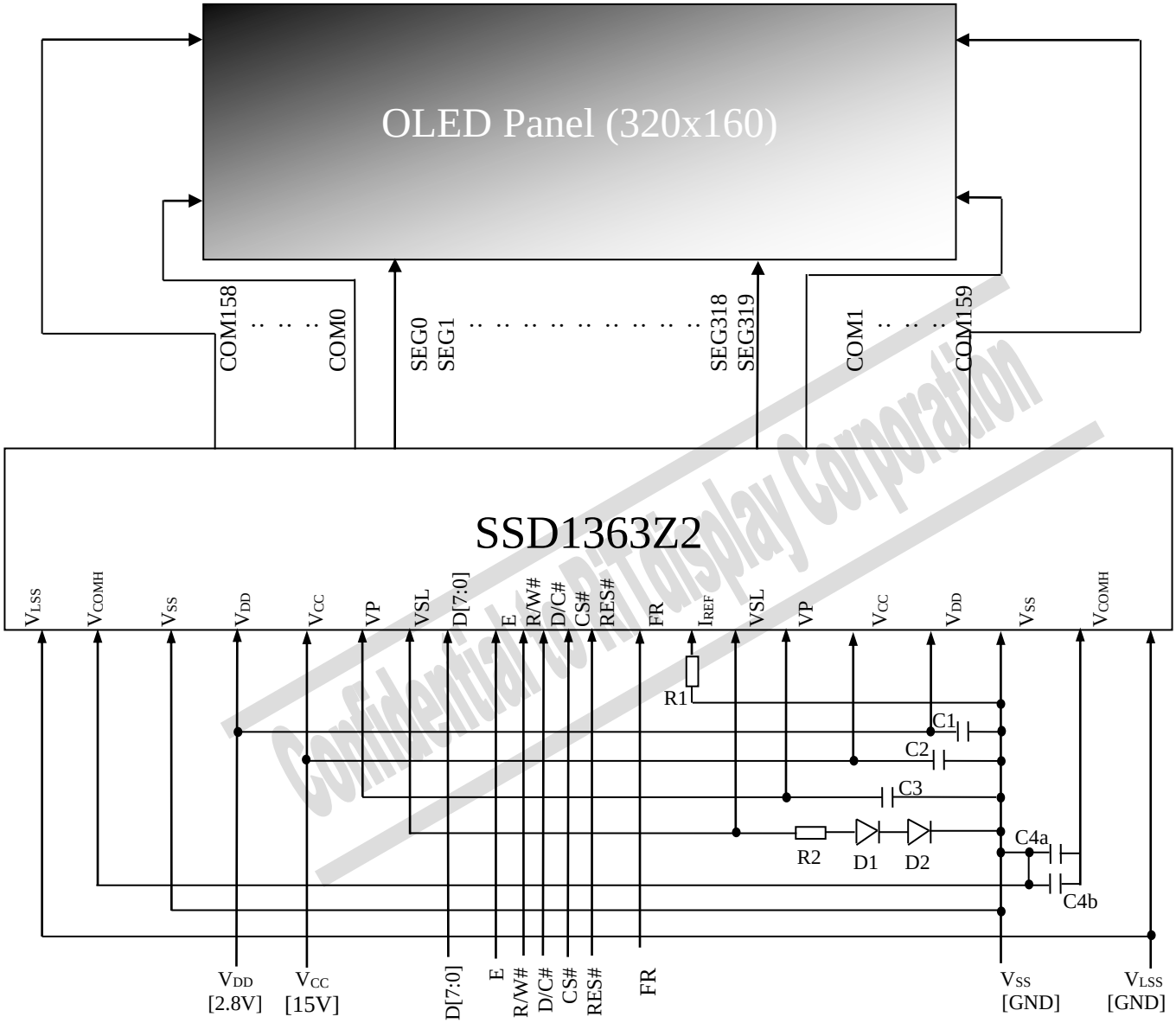
Figure 9-5 : I²C interface Timing characteristics



10 APPLICATION EXAMPLE

Figure 10-1 : SSD1363Z2 application example for 8080-parallel interface mode

The configuration for 8080-parallel interface mode is shown in the following diagram:
(V_{DD} = 2.8V, external V_{CC} = 15V, I_{REF} = 10uA

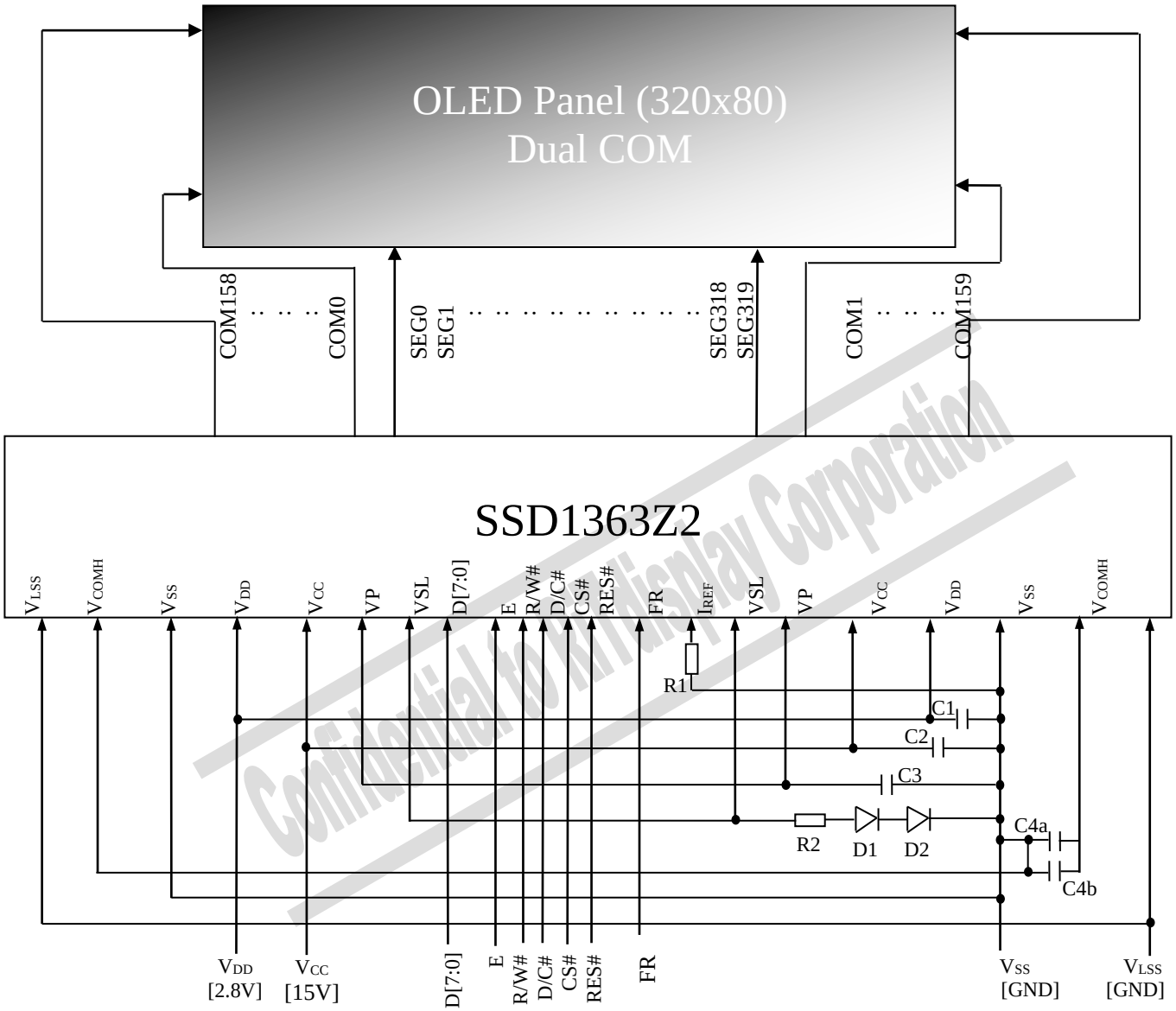


Pin connected to MCU interface: RES#, CS#, D/C#, R/W#(WR#), E(RD#)
Pin internally connected to V_{SS} / V_{LL}: BS0, CL_MS1, D_SEL, LS, BGGND, V_{SS1}
Pin internally connected to V_{DD} / V_{LH}: BS2, BS1, MS, CLS
Voltage at I_{REF} = V_{CC} – 2V. For V_{CC} = 15V, I_{REF} = 10uA:
R1 = (Voltage at I_{REF} - V_{SS}) / I_{REF}
= (15-2)V / 10uA = 1.3MΩ
R2 = 50Ω, 1/8W (1)
D1 ~ D2: V_{th}=0.7V, 1N4148 (1)
C1: 1uF, C3: 2.2uF, C2, C4a: 4.7uF, C3b: 0.1uF (1)

Note
(1) The capacitor value is recommended value. Select appropriate value against module application.
(2) All V_{LSS} pads of the IC are recommended to be connected together to form a larger area of GND.
(3) V_{LSS} and V_{SS} are not recommended to be connected on the ITO routing, but connected together in the PCB level at one common ground point for better grounding and noise insulation.

Figure 10-2 : SSD1363Z2 application example for 8080-parallel interface mode, dual COM mode

The configuration for 8080-parallel interface mode is shown in the following diagram:
(V_{DD} = 2.8V, external V_{CC} = 15V, I_{REF} = 10uA



Pin connected to MCU interface: RES#, CS#, D/C#, R/W#(WR#), E(RD#)
Pin internally connected to V_{SS} / V_{LL}: BS0, CL_MS1, D_SEL, LS, BGGND, V_{SS1}
Pin internally connected to V_{DD} / V_{LH}: BS2, BS1, MS, CLS
Voltage at I_{REF} = V_{CC} – 2V. For V_{CC} = 15V, I_{REF} = 10uA:
R1 = (Voltage at I_{REF} - V_{SS}) / I_{REF}
= (15-2)V / 10uA = 1.3MΩ
R2 = 50Ω, 1/8W (1)
D1 ~ D2: V_{th}=0.7V, 1N4148 (1)
C1: 1uF, C3: 2.2uF, C2, C4a: 4.7uF, C3b: 0.1uF (1)

Note
(1) The capacitor value is recommended value. Select appropriate value against module application.
(2) All V_{LSS} pads of the IC are recommended to be connected together to form a larger area of GND.
(3) V_{LSS} and V_{SS} are not recommended to be connected on the ITO routing, but connected together in the PCB level at one common ground point for better grounding and noise insulation.

The product(s) listed in this datasheet comply with Directive 2011/65/EU of the European Parliament and of the council of 8 June 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment and People’s Republic of China Electronic Industry Standard GB/T 26572-2011 “Requirements for concentration limits for certain hazardous substances in electronic information products (电子电器产品中限用物質的限用要求)”. Hazardous Substances test report is available upon request.

http://www.solomon-systech.com

Appendix III: SSD1363 Command Table

1 COMMAND TABLE

Table 1-1: SSD1363 Command Table

(D/C# = 0, R/W#(WR#)= 0, E(RD#) = 1) unless specific setting is stated
Single byte command (D/C# = 0), Multiple byte command (D/C# = 0 for first byte, D/C# = 1 for other bytes)

Fundamental Command Table											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0 1 1	15 A[7:0] B[7:0]	0 A_7 B_7	0 A_6 B_6	0 A_5 B_5	1 A_4 B_4	0 A_3 B_3	1 A_2 B_2	0 A_1 B_1	1 A_0 B_0	Set Column Address	A[7:0]: Start Address. [reset=0] B[7:0]: End Address. [reset=79d] Ranges from 0 to 79
0 1 1	75 A[7:0] B[7:0]	0 A_7 B_7	1 A_6 B_6	1 A_5 B_5	1 A_4 B_4	0 A_3 B_3	1 A_2 B_2	0 A_1 B_1	1 A_0 B_0	Set Row Address	A[7:0]: Start Address. [reset=0] B[7:0]: End Address. [reset=159d] Ranges from 0 to 159
0	5C	0	1	0	1	1	1	0	0	Write RAM Command	Enable MCU to write Data into RAM
0	5D	0	1	0	1	1	1	0	1	Read RAM Command	Enable MCU to read Data from RAM
0 1 1	A0 A[7:0] B[7:0]	1 * *	0 * *	1 A_5 *	0 A_4 B_4	0 A_3 *	0 * *	0 A_1 *	0 A_0 B_0	Set Re-map and Dual COM Line mode	A[0]=0b, Horizontal address increment [reset] A[0]=1b, Vertical address increment A[1]=0b, Column address 0 is mapped to SEG0 [reset] A[1]=1b, Column address 79 is mapped to SEG0 A[3]=0b, Reserved [reset] A[3]=1b, Reserved A[4]=0b, Scan from COM0 to COM[N –1] [reset] A[4]=1b, Scan from COM[N-1] to COM0. Where N is the Multiplex ratio. A[5]=0b, Disable COM Split Odd Even A[5]=1b, Enable COM Split Odd Even [reset] B[0] = 0b, Reserved [reset] B[0]=1b, Invalid B[4], Enable / disable Dual COM Line mode 0b, Disable Dual COM mode [reset] 1b, Enable Dual COM mode (MUX ≤ 79)
0 1	A1 A[7:0]	1 A_7	0 A_6	1 A_5	0 A_4	0 A_3	0 A_2	0 A_1	1 A_0	Set Display Start Line	Set vertical scroll by RAM from 0~159. [reset=00h]
0 1	A2 A[7:0]	1 A_7	0 A_6	1 A_5	0 A_4	0 A_3	0 A_2	1 A_1	0 A_0	Set Display Offset	Set vertical scroll by Row from 0-159. [reset=00h]

Fundamental Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	A4~A7	1	0	1	0	0	X_2	X_1	X_0	Set Display Mode	A4h: Entire Display OFF, all pixels turns OFF in GS level A5h: Entire Display ON, all pixels turns ON in GS level 15 A6h : Reset to normal display [reset] A7h: Inverse Display (GS0 -> GS15, GS1 -> GS14, ...)
0	AE~AF	1	0	1	0	1	1	1	X_0	Set Sleep mode ON/OFF	AEh = Sleep mode On (Display OFF) AFh = Sleep mode OFF (Display ON)
0 1	AD A[4]	1 1	0 0	1 0	0 A_4	1 0	1 0	0 0	1 0	Set Internal IREF	A[4] = 0b: Select external IREF [reset] A[4] = 1b: Enable internal IREF during display on
0 1	B1 A[7:0]	1 A_7	0 A_6	1 A_5	1 A_4	0 A_3	0 A_2	0 A_1	1 A_0	Set Reset (Phase 1) / Pre-charge (Phase 2) period	A[3:0] Phase 1 period of 1~15 DCLK(s) clocks [reset=0100b] A[3:0]: 0 invalid 1 = 1 DCLKs 2 = 2 DCLKs : 15 = 15DCLKs A[7:4] Phase 2 period of 1~15 DCLK(s) clocks [reset=0111b] A[7:4]: 0 invalid 1 = 1 DCLKs 2 = 2 DCLKs : 15 = 15DCLKs Note: (1) 0 DCLK is invalid in phase 1 & phase 2
0 1	B3 A[7:0]	1 A_7	0 A_6	1 A_5	1 A_4	0 A_3	0 A_2	1 A_1	1 A_0	Front Clock Divider (DivSet)/ Oscillator Frequency	A[3:0] [reset=0000b], divide by DIVSET where A[3:0] DIVSET 0000 divide by 1 0001 divide by 2 0010 divide by 3 0011 divide by 4 0100 divide by 5 : : 1011 divide by 11 1100 divide by 12 1101 divide by 13 1110 divide by 14 1111 divide by 15 A[7:4] Oscillator frequency, frequency increases as level increases [reset=0110b]

Fundamental Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	B6	1	0	1	1	0	1	0	0	Set Second Pre-charge Period	A[3:0] Set Second Pre-charge Period 0000b invalid 0001b 1 DCLKS 0010b 2 DCLKS : 1000 8 DCLKS [reset] : 1111 15 DCLKS
1	A[3:0]	1	1	0	0	A_3	A_2	A_1	A_0		
0	B8	1	0	1	1	1	0	0	0	Set Gray Scale Table	The next 15 data bytes define Gray Scale (GS) Table by setting the gray scale pulse width in unit of DCLK's (ranges from 0d ~ 180d) A1[7:0]: Gamma Setting for GS1, A2[7:0]: Gamma Setting for GS2, : : A14[7:0]: Gamma Setting for GS14, A15[7:0]: Gamma Setting for GS15 **Note** (1) 0 ≤ Setting of GS1 < Setting of GS2 < Setting of GS3..... < Setting of GS14 < Setting of GS15
1	A1[5:0]	0	0	$A1_5$	$A1_4$	$A1_3$	$A1_2$	$A1_1$	$A1_0$		
1	A2[5:0]	0	0	$A2_5$	$A2_4$	$A2_3$	$A2_2$	$A2_1$	$A2_0$		
1	.	.	.	.	.	.	.	.	.		
1	.	.	.	.	.	.	.	.	.		
1	.	.	.	.	.	.	.	.	.		
1	A14[5:0]	0	0	$A14_5$	$A14_4$	$A14_3$	$A14_2$	$A14_1$	$A14_0$		
1	A15[5:0]	0	0	$A15_5$	$A15_4$	$A15_3$	$A15_2$	$A15_1$	$A15_0$		
0	B9	1	0	1	1	1	0	0	1	Select Default Linear Gray Scale table [reset= linear]	The default Linear Gray Scale table is set in unit of DCLK's as follow GS0 level pulse width = 0; GS1 level pulse width = 4; GS2 level pulse width = 8; GS3 level pulse width = 12; : : GS14 level pulse width = 56; GS15 level pulse width = 60
0	BA	1	0	1	1	1	0	1	0	Set Pre-charge voltage configuration	Set pre-charge voltage configuration A[0]=0b, default when V_p pin is float in application [reset] A[0]=1b, external capacitance mode is enabled when V_p pin is connected to an external capacitor to GND in application
1	A[0]	0	0	0	0	0	0	1	A_0		
0	BB	1	0	1	1	1	0	1	1	Set Pre-charge voltage	Set pre-charge voltage level.[reset = 00111b] A[4:0] | Hex code | pre-charge voltage 00000 | 00h | 0.10 x V_{CC} : | : | : 00111 | 07h | 0.193 x V_{CC} [reset] : | : | : 11111 | 1Fh | 0.5133 x V_{CC} **Note** (1)Pre-charge voltage level must be smaller than COM deselect voltage level
1	A[4:0]	0	0	0	A_4	A_3	A_2	A_1	A_0		

Fundamental Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	BE	1	0	1	1	1	1	1	0	Set V_{COMH} Voltage	Set COM deselect voltage level [reset = 04h]
1	A[2:0]	0	0	0	0	0	A_2	A_1	A_0		

A[2:0]	Hex code	V_{COMH}
000	00h	0.72 x V_{CC}
:	:	:
100	04h	0.80 x V_{CC} [reset]
:	:	:
111	07h	0.86 x V_{CC}

0	C1	1	1	0	0	0	0	0	1	Set Contrast Current	A[7:0]: Contrast current value, ranges from 00h to FFh, i.e. 256 steps for I_{SEG} current [reset = 7Fh]
1	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	CA	1	1	0	0	1	0	1	0	Set MUX Ratio	A[6:0] MUX ratio 4MUX ~ 160MUX, [reset=159] (Ranges from 3 to 159)
1	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	FD	1	1	1	1	1	1	0	1	Set Command Lock	A[7:0]: MCU protection status [reset = 12h] A[7:0] = 12h, Unlock OLED driver IC MCU interface from entering command [reset] A[7:0] = 16h, Lock OLED driver IC MCU interface from entering command **Note** (1) The locked OLED driver IC MCU interface prohibits all commands and memory access except the FDh command.
1	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		

Note
(1) "*" stands for "Don't care".

Appendix IV: SSD1363 Command Description

1 COMMAND DESCRIPTION

1.1 Set Column Address (15h)

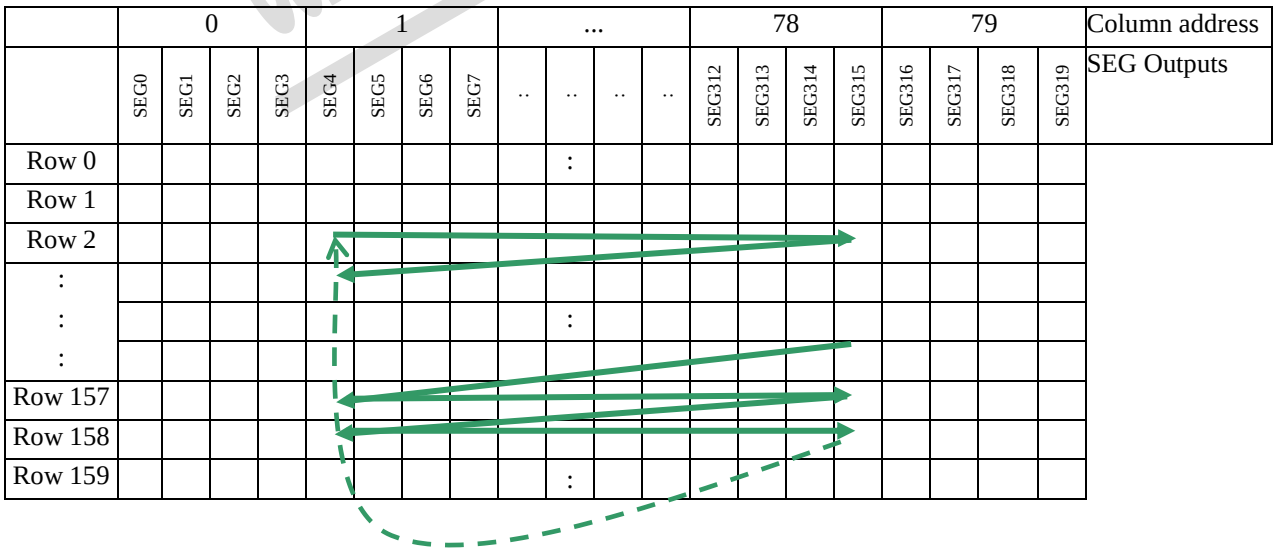
This triple byte command specifies column start address and end address of the display data RAM. This command also sets the column address pointer to column start address. This pointer is used to define the current read/write column address in graphic display data RAM. If horizontal address increment mode is enabled by command A0h, after finishing read/write one column data, it is incremented automatically to the next column address. Whenever the column address pointer finishes accessing the end column address, it is reset back to start column address and the row address is incremented to the next row.

1.2 Set Row Address (75h)

This triple byte command specifies row start address and end address of the display data RAM. This command also sets the row address pointer to row start address. This pointer is used to define the current read/write row address in graphic display data RAM. If vertical address increment mode is enabled by command A0h, after finishing read/write one row data, it is incremented automatically to the next row address. Whenever the row address pointer finishes accessing the end row address, it is reset back to start row address.

The diagram below shows the way of column and row address pointer movement through the example: column start address is set to 1 and column end address is set to 78, row start address is set to 2 and row end address is set to 158. Horizontal address increment mode is enabled by command A0h. In this case, the graphic display data RAM column accessible range is from column 1 to column 78 and from row 1 to row 158 only. In addition, the column and row address pointers are set to 1 and 2, respectively. After finishing read/write four pixels of data, the column address is increased automatically by 1 to access the next RAM location for next read/write operation (*solid line in Figure 1-1*). Whenever the column address pointer finishes accessing the end column 78, it is reset back to column 1 and row address is automatically increased by 1 (*solid line in Figure 1-1*). While the end row 158 and end column 78 RAM location is accessed, the row address is reset back to 2 and the column address is reset back to 1 (*dotted line in Figure 1-1*).

Figure 1-1 : Example of Column and Row Address Pointer Movement



1.3 Write RAM Command (5Ch)

After entering this single byte command, data entries will be written into the display RAM until another command is written. Address pointer is increased accordingly. This command must be sent before write data into RAM.

1.4 Read RAM Command (5Dh)

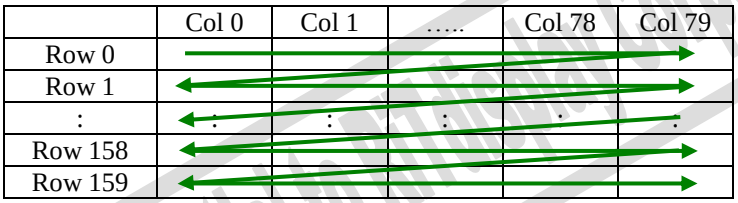
After entering this single byte command, data is read from display RAM until another command is written. Address pointer is increased accordingly. This command must be sent before read data from RAM.

1.5 Set Re-map / Color Depth (A0h)

This command has multiple configurations and each bit setting is described as follows:

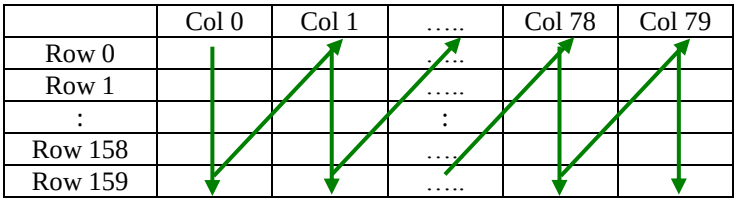
- Address increment mode (A[0])
  When A[0] is set to 0, the driver is set as horizontal address increment mode. After the display RAM is read / written, the column address pointer is increased automatically by 1. If the column address pointer reaches column end address, the column address pointer is reset to column start address and row address pointer is increased by 1. The sequence of movement of the row and column address point for horizontal address increment mode is shown in Figure 1-2.

Figure 1-2 : Address Pointer Movement of Horizontal Address Increment Mode



When A[0] is set to 1, the driver is set to vertical address increment mode. After the display RAM is read / written, the row address pointer is increased automatically by 1. If the row address pointer reaches the row end address, the row address pointer is reset to row start address and column address pointer is increased by 1. The sequence of movement of the row and column address point for vertical address increment mode is shown in Figure 1-3.

Figure 1-3: Address Pointer Movement of Vertical Address Increment Mode



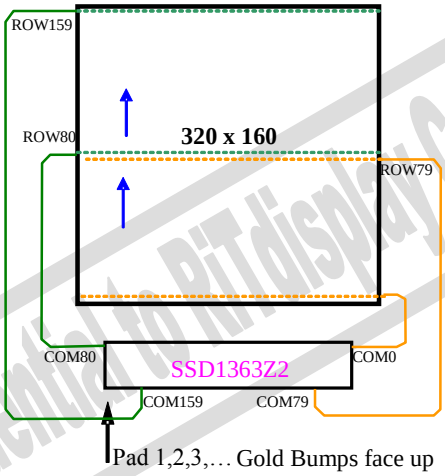
- Column Address Remap (A[1])
  This command bit is made for increasing the layout flexibility of segment signals in OLED module with segment arranged from left to right (when A[1] is set to 0) or vice versa (when A[1] is set to 1), as demonstrated in Figure 1-4.
  A[1] = 0 (reset): RAM Column 0 ~ 79 maps to SEG0-SEG3 ~ SEG316-SEG319
  A[1] = 1: RAM Column 0 ~ 79 maps to SEG316-SEG319 ~ SEG0-SEG3

- COM scan direction Remap (A[4])
  This command bit determines the scanning direction of the common for flexible layout of common signals in OLED module either from up to down or vice versa.
  A[4] = 0 (reset): COM scan from 0 to 159
  A[4] = 1: COM scan from 159 to 0
  Details of pin arrangement can be found in Figure 1-4.

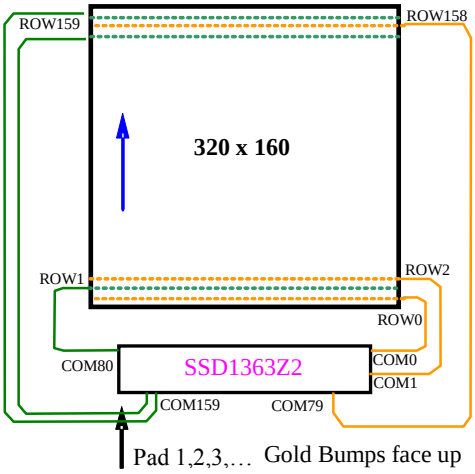
- Odd even split of COM pins (A[5])
  This command bit can set the odd even arrangement of COM pins.
  A[5] = 0 (reset): Disable COM split odd even, pin assignment of common is in sequential as
  COM159 COM158...COM 81 COM80...SEG319...SEG0...COM0 COM1...COM78 COM79
  A[5] = 1: Enable COM split odd even, pin assignment of common is in odd even split as
  COM159 COM157...COM3 COM1...SEG319...SEG0...COM0 COM2...COM156 COM158
  Details of pin arrangement can be found in Figure 1-4.

Figure 1-4 : COM Pins Hardware Configuration – 1 (MUX ratio: 160)

A[5] =0	A[4]=0
Disable Odd Even Split of COM pins	COM Scan Direction : from COM0 to COM159



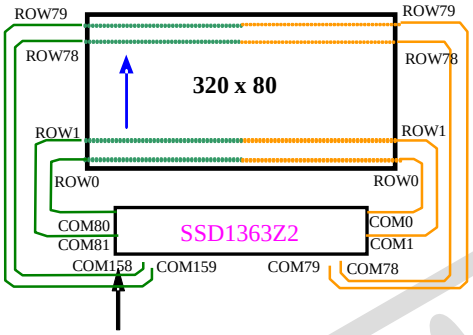
A[5] = 1	A[4] = 0
Enable Odd Even Split of COM pins	COM Scan Direction : from COM0 to COM159



- Set Dual COM mode (B[4])
  This command bit can set the dual COM mode.
  B[4] = 0 (reset): Disable the dual COM mode, as shown on Figure 1-4
  B[4] = 1: Enable the dual COM mode, details of pin arrangement can be found in Figure 1-5**Error! Reference source not found.**
  Notice that Odd even split of COM pins must be disabled (A[5]=0) and MUX must be set equating to or smaller than 79 (MUX≤79) when dual COM mode is enabled (B[4]=1).

Figure 1-5 : COM Pins Hardware Configuration – 2 (MUX ratio: 80)

A[5] = 0	B[4] = 1
Disable Odd Even Split of COM pins	Enable Dual COM mode



1.6 Set Display Start Line (A1h)

This command is used to set Display Start Line register to determine starting address of display RAM to be displayed by selecting a value from 0 to 159. Figure 1-6 shows an example of using this command when MUX ratio = 160 and MUX ratio = 96 and Display Start Line = 70. In there, "Row" means the graphic display data RAM row.

Figure 1-6 : Example of Set Display Start Line with no Remap

	MUX ratio (CAh) = 160	MUX ratio (CAh) = 160	MUX ratio (CAh) = 96	MUX ratio (CAh) = 96
COM Pin	Display Start Line (A1h) = 0	Display Start Line (A1h)= 70	Display Start Line (A1h) = 0	Display Start Line (A1h)= 70
COM0	ROW0	ROW70	ROW0	ROW70
COM1	ROW1	ROW71	ROW1	ROW71
COM2	ROW2	ROW72	ROW2	ROW72
COM3	ROW3	ROW73	ROW3	ROW73
:	:	:	:	:
:	:	:	:	:
COM23	ROW23	ROW93	ROW23	ROW93
COM24	ROW24	ROW94	ROW24	ROW94
COM25	ROW25	ROW95	ROW25	ROW95
COM26	ROW26	ROW96	ROW26	ROW96
COM27	ROW27	ROW97	ROW27	ROW97
:	:	:	:	:
:	:	:	:	:
COM88	ROW88	ROW158	ROW88	ROW158
COM89	ROW89	ROW159	ROW89	ROW159
COM90	ROW90	ROW0	ROW90	ROW0
COM91	ROW91	ROW1	ROW91	ROW1
COM92	ROW92	ROW2	ROW92	ROW2
COM93	ROW93	ROW3	ROW93	ROW3
COM94	ROW94	ROW4	ROW94	ROW4
COM95	ROW95	ROW5	ROW95	ROW5
COM96	ROW96	ROW6	-	-
COM97	ROW97	ROW7	-	-
:	:	:	:	:
:	:	:	:	:
COM156	ROW156	ROW66	-	-
COM157	ROW157	ROW67	-	-
COM158	ROW158	ROW68	-	-
COM159	ROW159	ROW69	-	-
Display Example				

1.7 Set Display Offset (A2h)

This command specifies the mapping of display start line (it is assumed that COM0 is the display start line, display start line register equals to 0) to one of COM0-159. For example, to move the COM69 towards the COM0 direction for 70 lines, the 7-bit data in the second command should be given by 01000110. Figure 1-7 below shows an example of this command. In there, "Row" means the graphic display data RAM row.

Figure 1-7 : Example of Set Display Offset with no Remap

	MUX ratio (CAh) = 160	MUX ratio (CAh) = 160	MUX ratio (CAh) = 96	MUX ratio (CAh) = 96
COM Pin	Display Offset (A2h) = 0	Display Offset (A2h) = 70	Display Offset (A2h) = 0	Display Offset (A2h) = 70
COM0	ROW0	ROW70	ROW0	ROW70
COM1	ROW1	ROW71	ROW1	ROW71
COM2	ROW2	ROW72	ROW2	ROW72
COM3	ROW3	ROW73	ROW3	ROW73
:	:	:	:	:
:	:	:	:	:
COM23	ROW23	ROW93	ROW23	ROW93
COM24	ROW24	ROW94	ROW24	ROW94
COM25	ROW25	ROW95	ROW25	ROW95
COM26	ROW26	ROW96	ROW26	-
COM27	ROW27	ROW97	ROW27	-
:	:	:	:	:
:	:	:	:	:
COM88	ROW88	ROW158	ROW88	-
COM89	ROW89	ROW159	ROW89	-
COM90	ROW90	ROW0	ROW90	ROW0
COM91	ROW91	ROW1	ROW91	ROW1
COM92	ROW92	ROW2	ROW92	ROW2
COM93	ROW93	ROW3	ROW93	ROW3
COM94	ROW94	ROW4	ROW94	ROW4
COM95	ROW95	ROW5	ROW95	ROW5
COM96	ROW96	ROW6	-	ROW6
COM97	ROW97	ROW7	-	ROW7
:	:	:	:	:
:	:	:	:	:
COM156	ROW156	ROW66	-	ROW66
COM157	ROW157	ROW67	-	ROW67
COM158	ROW158	ROW68	-	ROW68
COM159	ROW159	ROW69	-	ROW69
Display Example				

1.8 Set Display Mode (A4h ~ A7h)

These are single byte command and they are used to set Entire Display OFF, Entire Display ON, Normal Display and Inverse Display.

- Set Entire Display OFF (A4h)
  Force the entire display to be at gray scale level "GS0" regardless of the contents of the display data RAM as shown in Figure 1-8.

Figure 1-8 : Example of Entire Display OFF

GDDRAM Display

- Set Entire Display ON (A5h)
  Force the entire display to be at gray scale "GS15" regardless of the contents of the display data RAM as shown in Figure 1-9.

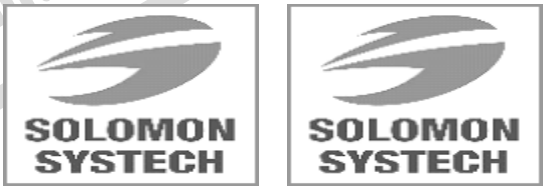
Figure 1-9 : Example of Entire Display ON

GDDRAM Display

- Normal Display (A6h)

  Reset the above effect and turn the data to ON at the corresponding gray level. Figure 1-10 shows an example of Normal Display.

Figure 1-10 : Example of Normal Display



GDDRAM Display

- Inverse Display (A7h)
  The gray level of display data are swapped such that "GS0" ↔ "GS15", "GS1" ↔ "GS14", …
  Figure 1-11 shows an example of inverse display

Figure 1-11 : Example of Inverse Display

GDDRAM Display

1.9 Set Sleep mode ON/OFF (AEh / AFh)

These single byte commands are used to turn the OLED panel display ON or OFF.

- When the display is ON (command AFh), the selected circuits by Set Master Configuration command will be turned ON.
- When the display is OFF (command AEh), the segment is in VSL state and common is in high impedance state.

1.10 Set Internal IREF (ADh)

This double byte command selects external IREF or internal IREF.

- When external IREF is selected (A[4]=0b), the magnitude of IREF is controlled by the value of resistor, which is connected between IREF pin and VSS. Details refer to Section 6.7 of Product Preview of SSD1363.
- When internal IREF is selected (A[4]=1b), the IREF pin should be kept NC.

1.11 Set Phase Length (B1h)

This double byte command sets the length of phase 1 and 2 of segment waveform of the driver.

- Phase 1 (A[3:0]): Set the period from 1 to 15 in the unit of 1 DCLK. A larger capacitance of the OLED pixel may require longer period to discharge the previous data charge completely.
- Phase 2 (A[7:4]): Set the period from 1 to 15 in the unit of 1 DCLK. A longer period is needed to charge up a larger capacitance of the OLED pixel to the target voltage V_P.

1.12 Set Front Clock Divider / Oscillator Frequency (B3h)

This double byte command consists of two functions:

- Front Clock Divide Ratio (A[3:0])
  Set the divide ratio to generate DCLK (Display Clock) from CLK. The divide ratio is from 1 to 16, with reset value = 1. Please refer to Product Preview Section 6.4 for the detail relationship of DCLK and CLK.

- Oscillator Frequency (A[7:4])
  Program the oscillator frequency Fosc which is the source of CLK if CLS pin is pulled HIGH. The 4-bit value results in 16 different frequency settings being available.

1.13 Set Second Pre-charge period (B6h)

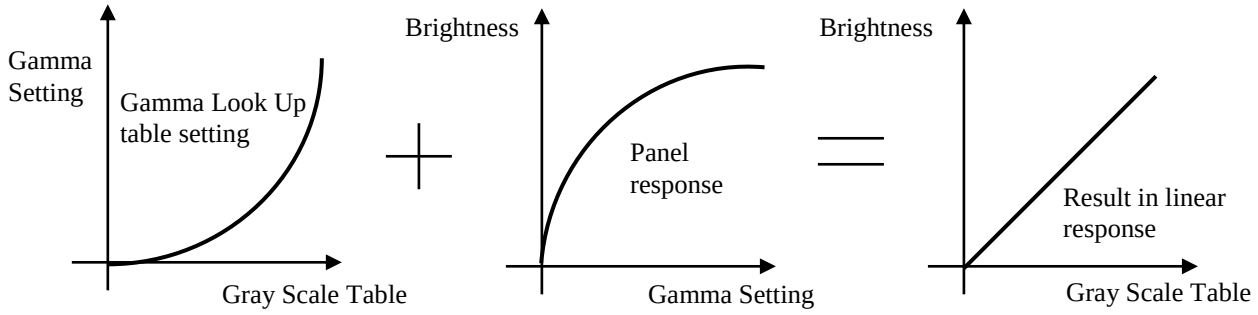
This double byte command is used to set the phase 3 second pre-charge period. The period of phase 3 can be programmed by command B6h and it is ranged from 1 to 15 DCLK's.

1.14 Set Gray Scale Table (B8h)

This command is used to set each individual gray scale level for the display. Except gray scale levels GS0 that has no pre-charge and current drive, each gray scale level is programmed in the length of current drive stage pulse width with unit of DCLK. The longer the length of the pulse width, the brighter the OLED pixel when it's turned ON. Following the command B8h, the user has to set the gray scale setting for GS1, GS2, …, GS14, GS15 one by one in sequence.

The setting of gray scale table entry can perform gamma correction on OLED panel display. Since the perception of the brightness scale shall match the image data value in display data RAM, appropriate gray scale table setting like the example shown below (Figure 1-12) can compensate this effect.

Figure 1-12: Example of Gamma correction by Gamma Look Up table setting



1.15 Select Default Linear Gray Scale Table (B9h)

This single byte command reloads the preset linear Gray Scale table. For color B, GS0 = Gamma Setting 0, GS1 = Gamma Setting 4, GS2 = Gamma Setting 8, GS3 = Gamma Setting 12,... GS14 = Gamma Setting 56, GS15 = Gamma Setting 60. Refer to Product Preview Section 6.9 for details.

1.16 Set Pre-charge voltage (BBh)

This double byte command sets the first pre-charge voltage (phase 2) level of segment pins. The level of pre-charge voltage is programmed with reference to V_{CC}.

1.17 Set V_{COMH} Voltage (BEh)

This double byte command sets the high voltage level of common pins, V_{COMH}. The level of V_{COMH} is programmed with reference to V_{CC}.

1.18 Set Contrast Current (C1h)

This command is used to set Contrast Setting of the display. The chip has 256 contrast steps from 00h to FFh. The segment output current I_{SEG} increases linearly with the contrast step, which results in brighter display.

1.19 Set Multiplex Ratio (CAh)

This double byte command switches default 1:160 multiplex mode to any multiplex mode from 4 to 160. For example, when multiplex ratio is set to 16, only 16 common pins are enabled. The starting and the ending of the enabled common pins are depended on the setting of "Display Offset" register programmed by command A2h. Figure 1-6 and Figure 1-7 show examples of setting the multiplex ratio through command CAh.

1.20 Set Command Lock (FDh)

This command is used to lock the OLED driver IC from accepting any command except itself. After entering FDh 16h (A[2]=1b), the OLED driver IC will not respond to any newly-entered command (except FDh 12h A[2]=0b) and there will be no memory access. This is call "Lock" state. That means the OLED driver IC ignore all the commands (except FDh 12h A[2]=0b) during the "Lock" state.

Entering FDh 12h (A[2]=0b) can unlock the OLED driver IC. That means the driver IC resume from the "Lock" state. And the driver IC will then respond to the command and memory access.