芯颖科技有限公司
CHIP WEALTH TECHNOLOGY LTD.

CH1120

160 X 160 16 Grayscale/Mono Dot Matrix OLED/PLED Driver with Controller

1. Features

- Support maximum 160×160 dots matrix panel with 16 grayscale and mono
- Support maximum 160×160 dots matrix panel with 1-bit mono mode
- Embedded 160×160 × 4 bits SRAM
- Operating voltage:
  - Logic voltage supply: V_{DD} = 1.65V – 3.5V
  - OLED Operating voltage supply: V_{PP} = 8.0V - 15V
- Maximum segment output current: 600μA
- Maximum common sink current: 96mA
- 8-bit 6800-series parallel interface, 8-bit 8080-series parallel interface
- 20MHz high speed 3-wire & 4-wire serial peripheral interface
- Programmable frame frequency and multiplexing ratio
- Horizontal and Vertical scroll
- Row re-mapping and column re-mapping
- Breathing Display Effect
- Internal or external I_{REF} selection
- VCOMH internal selection
- 256-step contrast control on monochrome passive OLED panel
- Low power consumption
  - Sleep mode:
  - VDD=1.65V – 2V, $I_{SP\_}$ V_{DD} < 10μA
  - VDD=2V – 3.5V, $I_{SP\_}$ V_{DD} < 15μA
  - $I_{SP\_}$ V_{PP} < 5μA
- Wide range of operating temperatures: -40 to +85°C
- Mono mode interface timing support
- Available in COG form

2. General Description

CH1120 is a single-chip CMOS OLED/PLED driver with controller for organic/polymer light emitting diode dot-matrix graphic display system. CH1120 consists of 160 segments, 160 commons with 16 grayscale that can support a maximum display resolution of 160 × 160. It is designed for Common Cathode type OLED panel.

CH1120 embeds with contrast control, display RAM oscillator. CH1120 is suitable for a wide range of compact portable applications, such as sub-display of mobile phone, calculator and MP3 player, etc.

3. Block Diagram

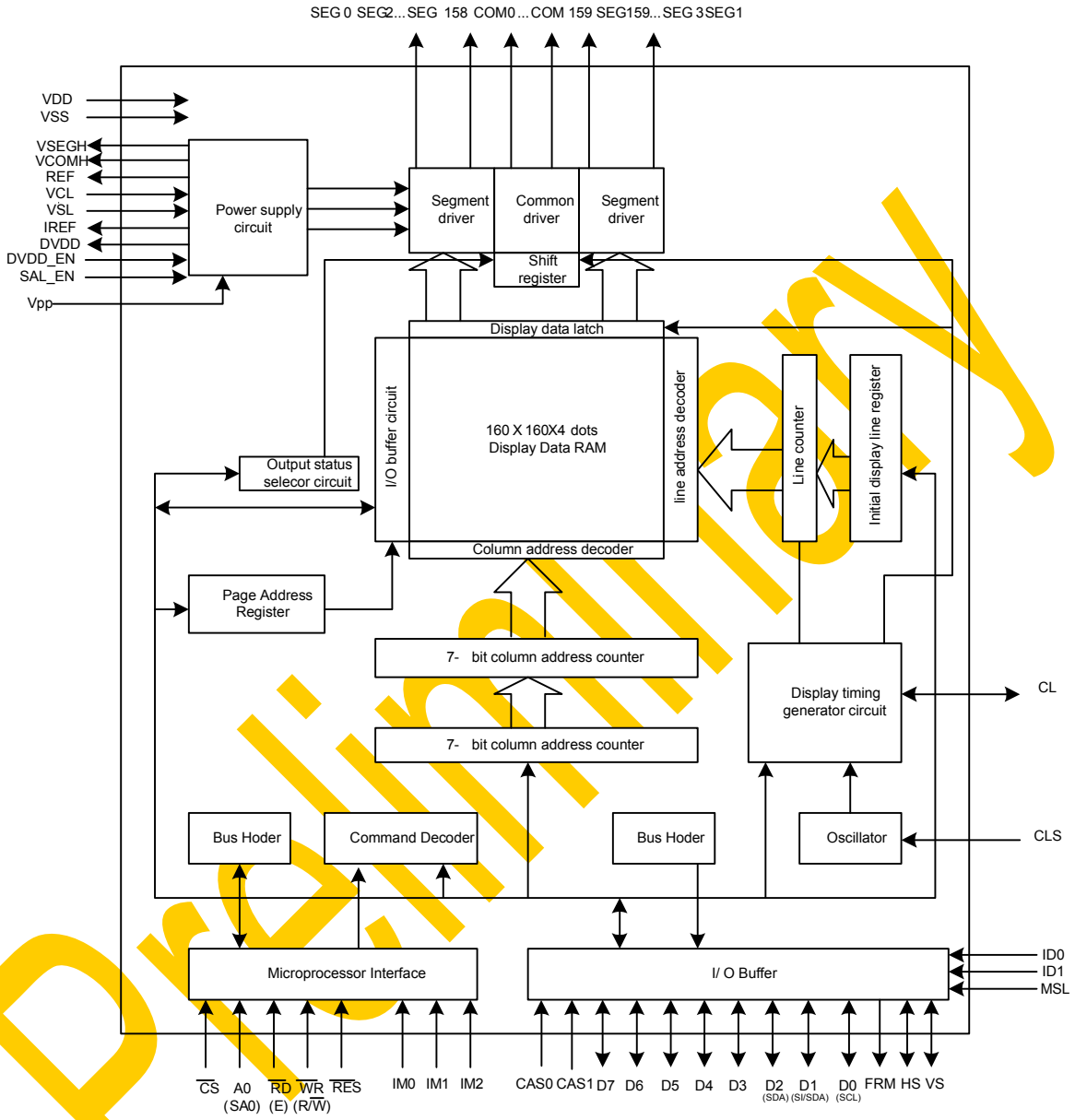


Figure 1 CH1120 Block Diagram

4. Pad Description

4.1. Power Supply

Pad NO.	Symbol	I/O	Description
29.33.53 57.61. 67~69	V_{DD}	Supply	1.65V– 3.5V Power supply for logic and input/output
18~21 31.38.51 55.59. 75~76	Vss (logic. analog)	Supply	Ground for logic and analog. This pad should be connected to GND externally. Two sides of VSS pads must be connected externally.
16~17 77~78	V_{SL}	Supply	Discharge voltage level pad. This pad should be connected to resistor and diode externally. Two sides of VSL pads must be connected externally.
22~26 70~74	V_{CL}	Supply	This is a common voltage reference pad. This pad should be connected to GND externally. Two sides of VCL pads must be connected externally.
6~9 89~92	V_{PP}	Supply	This is the most positive voltage supply pad of the chip It should be supplied externally. Two sides of VPP pads must be connected externally.

4.2. OLED Driver Supplies

Pad NO.	Symbol	I/O	Description
85	I_{REF}	O	This is a segment current reference pad. A resistor should be connected between this pad and GND.
10~13	V_{COMH}	O	This is a pad for the voltage output high level for common signals. A capacitor should be connected between this pad and GND.
65~66	DVDD	O	This pin is for regulator circuit. A capacitor should be connected between this pad and GND if necessary. When external capacitor Is not used, this pin should be kept NC.
14~15	VSEGH	O	This is a segment pre-charge voltage. A capacitor can be connected between this pad and GND if necessary. When external capacitor Is not used, this pin should be kept NC on FPC.

4.3. System Bus Connection Pads

<table>
<tr><th>Symbol</th><th>I/O</th><th>Description</th></tr>
<tr><td>CL</td><td>I/O</td><td>This pad is the system clock input. When internal clock is enabled, this pad should be left open. The internal clock is output from this pad. When internal oscillator is disabled, this pad receives display clock signal from external clock source.</td></tr>
<tr><td>CLS</td><td>I</td><td>This is the internal clock enable pad.
CLS = “H”: Internal oscillator circuit is enabled.
CLS = “L”: Internal oscillator circuit is disabled (requires external input).
When CLS = “L”, an external clock source must be connected to the CL pad for normal operation.
This pin internal pull high.</td></tr>
<tr><td>IM0
IM1
IM2</td><td>I</td><td>These are the MPU interface mode select pads.
<table>
<tr><td></td><td>8080</td><td>3-wire SPI</td><td>4-wire SPI</td><td>6800</td><td>I^{2}C</td></tr>
<tr><td>IM0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>IM1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>IM2</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td></tr>
</table>
These pins must be connected to “H” or “L”.</td></tr>
<tr><td>ID0
ID1</td><td>I</td><td>These pins are Panel ID setting for customers use. Customers can connect these pins to H or L through read register E1h to confirm which panel and send corresponding initial code. These pins must be connected to “H” or “L”.
<table>
<tr><td></td><td>Panel ID1</td><td>Panel ID2</td><td>Panel ID3</td><td>Panel ID4</td></tr>
<tr><td>ID0</td><td>0</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>ID1</td><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>E1h</td><td>0x00</td><td>0x01</td><td>0x02</td><td>0x03</td></tr>
</table></td></tr>
<tr><td>DVDD
_EN</td><td>I</td><td>This pin should be connected to “H” to turn on regulator for digital circuit. When VDD <1.98V, writing this CMD to turn off the DVDD regulator circuit for avoiding more static current generated on VDD. The relation between DVDD_EN hardware pin and DVDD regulator off command is as below:
<table>
<tr><td>DVDD_ EN
Hardware pin</td><td>DVDD regulator off
Command</td><td>Result</td></tr>
<tr><td>1</td><td>0 (5A.A5.AA)</td><td>0 (Regulator OFF)</td></tr>
<tr><td>1</td><td>1 (default,00.00.00)</td><td>1 (Regulator ON)</td></tr>
</table>
This pin must be connected to “H”.</td></tr>
<tr><td>SAL_EN</td><td>I</td><td>Bandgap/DVDD regulater lowpower mode hardware pin control.
SAL_EN = H : Enable (default) This pin internal pull high.
SAL_EN = L : Disable</td></tr>
<tr><td>CSB</td><td>I</td><td>This pad is the chip select input. When CSB = “L”, then the chip select becomes active,
and data/command I/O is enabled.
When in I2C interface , this pin is not used, so it must be connected to “L”.</td></tr>
<tr><td>RESB</td><td>I</td><td>This is a reset signal input pad. When RESB is set to “L”, the settings are initialized. The reset operation is performed by the RESB signal level. This pin internal pull high.</td></tr>
</table>

<table>
<tr><td>A0
（SA0）</td><td>I</td><td>This is the Data/Command control pad that determines whether the data bits are data or a command.
A0 = “H”: the inputs at D0 to D7 are treated as display data.
A0 = “L”: the inputs at D0 to D7 are transferred to the command registers.
In I^2C interface, this pad serves as SA0 to distinguish the different address of OLED driver.
When in 3-wire interface , this pin is not used, so it must be connected to “L”.</td></tr>
<tr><td>WRB
(R/$\overline{W}$)</td><td>I</td><td>This is a MPU interface input pad.
When connected to an 8080 MPU, this is active LOW. This pad connects to the 8080 MPU $\overline{WR}$ signal. The signals on the data bus are latched at the rising edge of the $\overline{WR}$ signal.
When connected to a 6800 Series MPU: This is the read/write control signal input terminal.
When R/$\overline{W}$ = “H”: Read.
When R/$\overline{W}$ = “L”: Write.
When in 3-wire.4-wire & I2C interface , this pin is not used, so it must be connected to “L”.</td></tr>
<tr><td>RDB
(E)</td><td>I</td><td>This is a MPU interface input pad.
When connected to an 8080 series MPU, it is active LOW. This pad is connected to the $\overline{RD}$ signal of the 8080 series MPU, and the data bus is in an output status when this signal is “L”.
When connected to a 6800 series MPU, this is active HIGH. This is used as an enable clock input of the 6800 series MPU.
When in 3-wire.4-wire & I2C interface , this pin is not used, so it must be connected to “L”.</td></tr>
<tr><td>D0 - D7
(SCL)
(SI/SDA)</td><td>I/O
I
I/O</td><td>This is an 8-bit bi-directional data bus that connects to an 8-bit or 16-bit standard MPU data bus.
When the serial interface(SPI) and I2C is selected, then D0 serves as the serial clock input pad (SCL) and D1 serves as the serial data input pad (SI). At this time, D2 to D7 are set to high impedance. D7~D2 is recommended to connect the VDD or GND. It is also allowed to leave D7~D2 unconnected.</td></tr>
<tr><td>FRM</td><td>O</td><td>This pad is No Connection pad, Its signal varies with the frame frequency. Its voltage is equal to VDD when the last common output of every frame is active, and is equal to GND during other time.</td></tr>
<tr><td>HS_L</td><td>I/O</td><td>Test pad, no connection for user.</td></tr>
<tr><td>VS_L</td><td>I/O</td><td>Test pad, no connection for user.</td></tr>
<tr><td>CLK_L</td><td>I/O</td><td>Test pad, no connection for user.</td></tr>
<tr><td>HS_R</td><td>I/O</td><td>Test pad, no connection for user.</td></tr>
<tr><td>VS_R</td><td>I/O</td><td>Test pad, no connection for user.</td></tr>
<tr><td>CLK_R</td><td>I/O</td><td>Test pad, no connection for user.</td></tr>
<tr><td>MSL</td><td>I</td><td>This pin sets master or slave.
When MSL=”H”, it is a Master IC.
When MSL=”L”, it is a Slave IC.
<table>
<tr><th>MSL</th><th>Mode</th></tr>
<tr><td>0</td><td>Slave</td></tr>
<tr><td>1</td><td>Master</td></tr>
</table>
This pin internal pull high.</td></tr>
<tr><td>CAS0
CAS1</td><td>I</td><td>These pins must be connected to “L”.
<table>
<tr><th>CAS1</th><th>CAS0</th><th>Mode</th></tr>
<tr><td>0</td><td>0</td><td>Normal</td></tr>
</table></td></tr>
</table>

REF	O	Test pad, no connection for user.

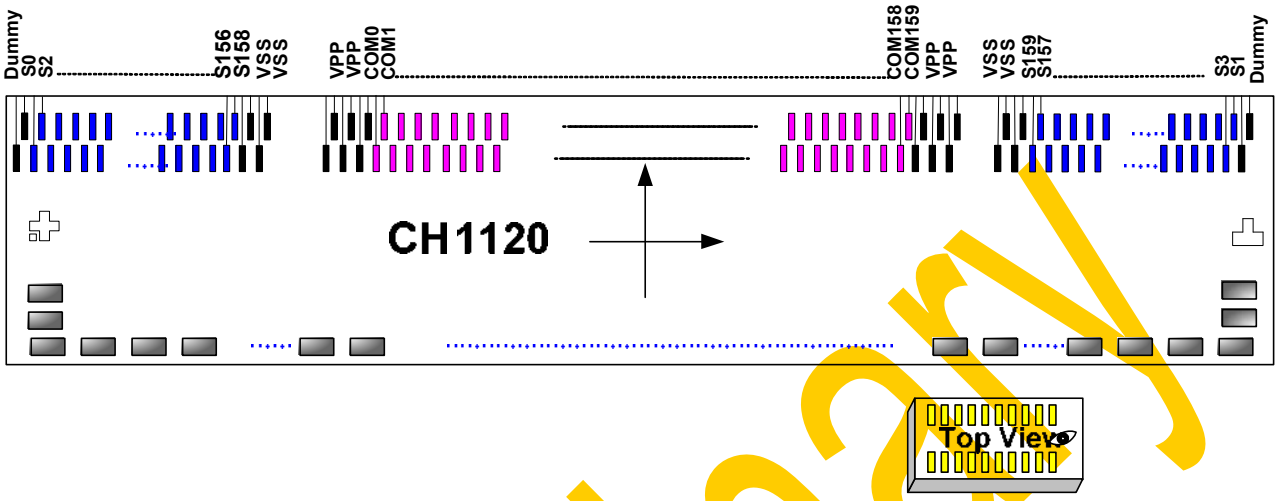
4.4. OLED Drive Pads

Symbol	I/O	Description
SEG0,2, - 158	O	These pads are even Segment signal output for OLED display.
SEG1,3 -159	O	These pads are odd Segment signal output for OLED display.
COM0 - 159	O	These pads are Common signal output for OLED display.

4.5. Test Pads

Symbol	I/O	Description
TEST1	I/O	Test pad, no connection for user.
TEST2	I/O	Test pad, no connection for user.
TEST3	I/O	Test pad, no connection for user.
TEST4	I/O	Test pad, no connection for user.
TEST5	I/O	Test pad, no connection for user.
TEST6	I/O	Test pad, no connection for user.
TEST7	I/O	Test pad, no connection for user.
TEST8	I/O	Test pad, no connection for user.
TEST9	I/O	Test pad, no connection for user.
Dummy	-	Dummy pads, no connection for user

5. Pad Configuration



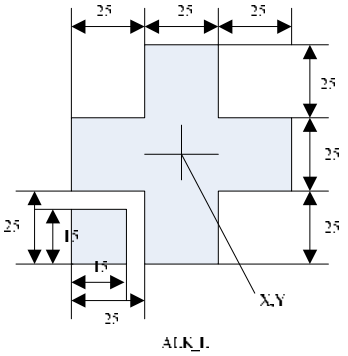
5.1. Chip Outline Dimensions

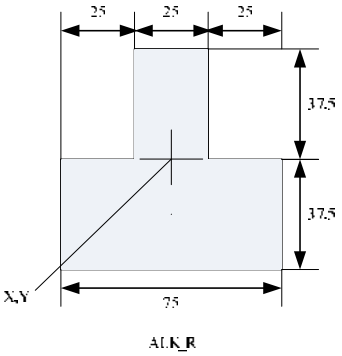
Item	Pad No.	Size (μm)	
		X	Y
Chip boundary	-	8628	728
Chip height	All pads	250	
Bump size	I/O	76.5	52
	SEG	13	93
	COM	13	103
Pad pitch	COM	49	
	SEG	49	
	I/O	91.5	
Bump height	All pads	9±2	

5.2. Alignment Mark Location

Unit: μm

NO	X	Y
ALK_L	-4215.5	-77
ALK_R	4215.5	-77





5.3. Pad Location (Total: 441 pads)

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y	Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
1	DUMMY1	-4209	-173	71	vcl	2013	-277.3	141	SEG[83]	3196	98	211	COM[138]	1433.25	80.5
2	DUMMY1	-4209	-220	72	vcl	2104.5	-277.3	142	SEG[85]	3171.5	238	212	COM[137]	1408.75	225.5
3	hs_L	-4209	-277.3	73	vcl	2196	-277.3	143	SEG[87]	3147	98	213	COM[136]	1384.25	80.5
4	vs_L	-4117.5	-277.3	74	vcl	2287.5	-277.3	144	SEG[89]	3122.5	238	214	COM[135]	1359.75	225.5
5	clk_L	-4026	-277.3	75	vss	2379	-277.3	145	SEG[91]	3098	98	215	COM[134]	1335.25	80.5
6	vpp	-3934.5	-277.3	76	vss	2470.5	-277.3	146	SEG[93]	3073.5	238	216	COM[133]	1310.75	225.5
7	vpp	-3843	-277.3	77	vsl	2562	-277.3	147	SEG[95]	3049	98	217	COM[132]	1286.25	80.5
8	vpp	-3751.5	-277.3	78	vsl	2653.5	-277.3	148	SEG[97]	3024.5	238	218	COM[131]	1261.75	225.5
9	vpp	-3660	-277.3	79	test2	2745	-277.3	149	SEG[99]	3000	98	219	COM[130]	1237.25	80.5
10	vcomh	-3568.5	-277.3	80	test3	2836.5	-277.3	150	SEG[101]	2975.5	238	220	COM[129]	1212.75	225.5
11	vcomh	-3477	-277.3	81	test4	2928	-277.3	151	SEG[103]	2951	98	221	COM[128]	1188.25	80.5
12	vcomh	-3385.5	-277.3	82	test5	3019.5	-277.3	152	SEG[105]	2926.5	238	222	COM[127]	1163.75	225.5
13	vcomh	-3294	-277.3	83	test6	3111	-277.3	153	SEG[107]	2902	98	223	COM[126]	1139.25	80.5
14	vsegh	-3202.5	-277.3	84	test7	3202.5	-277.3	154	SEG[109]	2877.5	238	224	COM[125]	1114.75	225.5
15	vsegh	-3111	-277.3	85	iref	3294	-277.3	155	SEG[111]	2853	98	225	COM[124]	1090.25	80.5
16	vsl	-3019.5	-277.3	86	REF	3385.5	-277.3	156	SEG[113]	2828.5	238	226	COM[123]	1065.75	225.5
17	vsl	-2928	-277.3	87	test8	3477	-277.3	157	SEG[115]	2804	98	227	COM[122]	1041.25	80.5
18	vss	-2836.5	-277.3	88	test9	3568.5	-277.3	158	SEG[117]	2779.5	238	228	COM[121]	1016.75	225.5
19	vss	-2745	-277.3	89	vpp	3660	-277.3	159	SEG[119]	2755	98	229	COM[120]	992.25	80.5
20	vss	-2653.5	-277.3	90	vpp	3751.5	-277.3	160	SEG[121]	2730.5	238	230	COM[119]	967.75	225.5
21	vss	-2562	-277.3	91	vpp	3843	-277.3	161	SEG[123]	2706	98	231	COM[118]	943.25	80.5
22	vcl	-2470.5	-277.3	92	vpp	3934.5	-277.3	162	SEG[125]	2681.5	238	232	COM[117]	918.75	225.5
23	vcl	-2379	-277.3	93	clk_R	4026	-277.3	163	SEG[127]	2657	98	233	COM[116]	894.25	80.5
24	vcl	-2287.5	-277.3	94	vs_R	4117.5	-277.3	164	SEG[129]	2632.5	238	234	COM[115]	869.75	225.5
25	vcl	-2196	-277.3	95	hs_R	4209	-277.3	165	SEG[131]	2608	98	235	COM[114]	845.25	80.5
26	vcl	-2104.5	-277.3	96	DUMMY2	4209	-220	166	SEG[133]	2583.5	238	236	COM[113]	820.75	225.5
27	test1	-2013	-277.3	97	DUMMY2	4209	-173	167	SEG[135]	2559	98	237	COM[112]	796.25	80.5
28	test1	-1921.5	-277.3	98	DUMMY_VSS[1]	4249.5	238	168	SEG[137]	2534.5	238	238	COM[111]	771.75	225.5
29	vdd	-1830	-277.3	99	DUMMY_VSS[2]	4225	98	169	SEG[139]	2510	98	239	COM[110]	747.25	80.5
30	id0	-1738.5	-277.3	100	SEG[1]	4200.5	238	170	SEG[141]	2485.5	238	240	COM[109]	722.75	225.5
31	vss	-1647	-277.3	101	SEG[3]	4176	98	171	SEG[143]	2461	98	241	COM[108]	698.25	80.5
32	id1	-1555.5	-277.3	102	SEG[5]	4151.5	238	172	SEG[145]	2436.5	238	242	COM[107]	673.75	225.5
33	vdd	-1464	-277.3	103	SEG[7]	4127	98	173	SEG[147]	2412	98	243	COM[106]	649.25	80.5
34	cl	-1372.5	-277.3	104	SEG[9]	4102.5	238	174	SEG[149]	2387.5	238	244	COM[105]	624.75	225.5
35	frm	-1281	-277.3	105	SEG[11]	4078	98	175	SEG[151]	2363	98	245	COM[104]	600.25	80.5
36	resb	-1189.5	-277.3	106	SEG[13]	4053.5	238	176	SEG[153]	2338.5	238	246	COM[103]	575.75	225.5
37	a0	-1098	-277.3	107	SEG[15]	4029	98	177	SEG[155]	2314	98	247	COM[102]	551.25	80.5
38	vss	-1006.5	-277.3	108	SEG[17]	4004.5	238	178	SEG[157]	2289.5	238	248	COM[101]	526.75	225.5
39	wrb	-915	-277.3	109	SEG[19]	3980	98	179	SEG[159]	2265	98	249	COM[100]	502.25	80.5
40	rdb	-823.5	-277.3	110	SEG[21]	3955.5	238	180	DUMMY_VSS[5]	2240.5	238	250	COM[99]	477.75	225.5
41	csb	-732	-277.3	111	SEG[23]	3931	98	181	DUMMY_VSS[6]	2216	98	251	COM[98]	453.25	80.5
42	d[0]	-640.5	-277.3	112	SEG[25]	3906.5	238	182	DUMMY_VSS[7]	2191.5	238	252	COM[97]	428.75	225.5
43	d[1]	-549	-277.3	113	SEG[27]	3882	98	183	DUMMY_VSS[8]	2167	98	253	COM[96]	404.25	80.5
44	d[2]	-457.5	-277.3	114	SEG[29]	3857.5	238	184	DUMMY_VPP[1]	2094.75	225.5	254	COM[95]	379.75	225.5
45	d[3]	-366	-277.3	115	SEG[31]	3833	98	185	DUMMY_VPP[2]	2070.25	80.5	255	COM[94]	355.25	80.5
46	d[4]	-274.5	-277.3	116	SEG[33]	3808.5	238	186	DUMMY_VPP[3]	2045.75	225.5	256	COM[93]	330.75	225.5
47	d[5]	-183	-277.3	117	SEG[35]	3784	98	187	DUMMY_VPP[4]	2021.25	80.5	257	COM[92]	306.25	80.5
48	d[6]	-91.5	-277.3	118	SEG[37]	3759.5	238	188	DUMMY_VPP[5]	1996.75	225.5	258	COM[91]	281.75	225.5
49	d[7]	0	-277.3	119	SEG[39]	3735	98	189	DUMMY_VPP[6]	1972.25	80.5	259	COM[90]	257.25	80.5
50	msl	91.5	-277.3	120	SEG[41]	3710.5	238	190	COM[159]	1947.75	225.5	260	COM[89]	232.75	225.5
51	vss	183	-277.3	121	SEG[43]	3686	98	191	COM[158]	1923.25	80.5	261	COM[88]	208.25	80.5
52	im1	274.5	-277.3	122	SEG[45]	3661.5	238	192	COM[157]	1898.75	225.5	262	COM[87]	183.75	225.5
53	vdd	366	-277.3	123	SEG[47]	3637	98	193	COM[156]	1874.25	80.5	263	COM[86]	159.25	80.5
54	im2	457.5	-277.3	124	SEG[49]	3612.5	238	194	COM[155]	1849.75	225.5	264	COM[85]	134.75	225.5
55	vss	549	-277.3	125	SEG[51]	3588	98	195	COM[154]	1825.25	80.5	265	COM[84]	110.25	80.5
56	im0	640.5	-277.3	126	SEG[53]	3563.5	238	196	COM[153]	1800.75	225.5	266	COM[83]	85.75	225.5
57	vdd	732	-277.3	127	SEG[55]	3539	98	197	COM[152]	1776.25	80.5	267	COM[82]	61.25	80.5
58	cas0	823.5	-277.3	128	SEG[57]	3514.5	238	198	COM[151]	1751.75	225.5	268	COM[81]	36.75	225.5
59	vss	915	-277.3	129	SEG[59]	3490	98	199	COM[150]	1727.25	80.5	269	COM[80]	12.25	80.5
60	cas1	1006.5	-277.3	130	SEG[61]	3465.5	238	200	COM[149]	1702.75	225.5	270	COM[79]	-12.25	225.5
61	vdd	1098	-277.3	131	SEG[63]	3441	98	201	COM[148]	1678.25	80.5	271	COM[78]	-36.75	80.5
62	dvdd_en	1189.5	-277.3	132	SEG[65]	3416.5	238	202	COM[147]	1653.75	225.5	272	COM[77]	-61.25	225.5
63	sal_en	1281	-277.3	133	SEG[67]	3392	98	203	COM[146]	1629.25	80.5	273	COM[76]	-85.75	80.5
64	cls	1372.5	-277.3	134	SEG[69]	3367.5	238	204	COM[145]	1604.75	225.5	274	COM[75]	-110.25	225.5
65	dvdd	1464	-277.3	135	SEG[71]	3343	98	205	COM[144]	1580.25	80.5	275	COM[74]	-134.75	80.5
66	dvdd	1555.5	-277.3	136	SEG[73]	3318.5	238	206	COM[143]	1555.75	225.5	276	COM[73]	-159.25	225.5
67	vdd	1647	-277.3	137	SEG[75]	3294	98	207	COM[142]	1531.25	80.5	277	COM[72]	-183.75	80.5
68	vdd	1738.5	-277.3	138	SEG[77]	3269.5	238	208	COM[141]	1506.75	225.5	278	COM[71]	-208.25	225.5
69	vdd	1830	-277.3	139	SEG[79]	3245	98	209	COM[140]	1482.25	80.5	279	COM[70]	-232.75	80.5
70	vcl	1921.5	-277.3	140	SEG[81]	3220.5	238	210	COM[139]	1457.75	225.5	280	COM[69]	-257.25	225.5

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y	Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
281	COM[68]	-281.75	80.5	346	COM[3]	-1874.25	225.5	411	SEG[56]	-3514.5	98				
282	COM[67]	-306.25	225.5	347	COM[2]	-1898.75	80.5	412	SEG[54]	-3539	238				
283	COM[66]	-330.75	80.5	348	COM[1]	-1923.25	225.5	413	SEG[52]	-3563.5	98				
284	COM[65]	-355.25	225.5	349	COM[0]	-1947.75	80.5	414	SEG[50]	-3588	238				
285	COM[64]	-379.75	80.5	350	DUMMY_VPP[7]	-1972.25	225.5	415	SEG[48]	-3612.5	98				
286	COM[63]	-404.25	225.5	351	DUMMY_VPP[8]	-1996.75	80.5	416	SEG[46]	-3637	238				
287	COM[62]	-428.75	80.5	352	DUMMY_VPP[9]	-2021.25	225.5	417	SEG[44]	-3661.5	98				
288	COM[61]	-453.25	225.5	353	DUMMY_VPP[10]	-2045.75	80.5	418	SEG[42]	-3686	238				
289	COM[60]	-477.75	80.5	354	DUMMY_VPP[11]	-2070.25	225.5	419	SEG[40]	-3710.5	98				
290	COM[59]	-502.25	225.5	355	DUMMY_VPP[12]	-2094.75	80.5	420	SEG[38]	-3735	238				
291	COM[58]	-526.75	80.5	356	DUMMY_VSS[9]	-2167	238	421	SEG[36]	-3759.5	98				
292	COM[57]	-551.25	225.5	357	DUMMY_VSS[10]	-2191.5	98	422	SEG[34]	-3784	238				
293	COM[56]	-575.75	80.5	358	DUMMY_VSS[11]	-2216	238	423	SEG[32]	-3808.5	98				
294	COM[55]	-600.25	225.5	359	DUMMY_VSS[12]	-2240.5	98	424	SEG[30]	-3833	238				
295	COM[54]	-624.75	80.5	360	SEG[158]	-2265	238	425	SEG[28]	-3857.5	98				
296	COM[53]	-649.25	225.5	361	SEG[156]	-2289.5	98	426	SEG[26]	-3882	238				
297	COM[52]	-673.75	80.5	362	SEG[154]	-2314	238	427	SEG[24]	-3906.5	98				
298	COM[51]	-698.25	225.5	363	SEG[152]	-2338.5	98	428	SEG[22]	-3931	238				
299	COM[50]	-722.75	80.5	364	SEG[150]	-2363	238	429	SEG[20]	-3955.5	98				
300	COM[49]	-747.25	225.5	365	SEG[148]	-2387.5	98	430	SEG[18]	-3980	238				
301	COM[48]	-771.75	80.5	366	SEG[146]	-2412	238	431	SEG[16]	-4004.5	98				
302	COM[47]	-796.25	225.5	367	SEG[144]	-2436.5	98	432	SEG[14]	-4029	238				
303	COM[46]	-820.75	80.5	368	SEG[142]	-2461	238	433	SEG[12]	-4053.5	98				
304	COM[45]	-845.25	225.5	369	SEG[140]	-2485.5	98	434	SEG[10]	-4078	238				
305	COM[44]	-869.75	80.5	370	SEG[138]	-2510	238	435	SEG[8]	-4102.5	98				
306	COM[43]	-894.25	225.5	371	SEG[136]	-2534.5	98	436	SEG[6]	-4127	238				
307	COM[42]	-918.75	80.5	372	SEG[134]	-2559	238	437	SEG[4]	-4151.5	98				
308	COM[41]	-943.25	225.5	373	SEG[132]	-2583.5	98	438	SEG[2]	-4176	238				
309	COM[40]	-967.75	80.5	374	SEG[130]	-2608	238	439	SEG[0]	-4200.5	98				
310	COM[39]	-992.25	225.5	375	SEG[128]	-2632.5	98	440	DUMMY_VSS[3]	-4225	238				
311	COM[38]	-1016.75	80.5	376	SEG[126]	-2657	238	441	DUMMY_VSS[4]	-4249.5	98				
312	COM[37]	-1041.25	225.5	377	SEG[124]	-2681.5	98								
313	COM[36]	-1065.75	80.5	378	SEG[122]	-2706	238								
314	COM[35]	-1090.25	225.5	379	SEG[120]	-2730.5	98								
315	COM[34]	-1114.75	80.5	380	SEG[118]	-2755	238								
316	COM[33]	-1139.25	225.5	381	SEG[116]	-2779.5	98								
317	COM[32]	-1163.75	80.5	382	SEG[114]	-2804	238								
318	COM[31]	-1188.25	225.5	383	SEG[112]	-2828.5	98								
319	COM[30]	-1212.75	80.5	384	SEG[110]	-2853	238								
320	COM[29]	-1237.25	225.5	385	SEG[108]	-2877.5	98								
321	COM[28]	-1261.75	80.5	386	SEG[106]	-2902	238								
322	COM[27]	-1286.25	225.5	387	SEG[104]	-2926.5	98								
323	COM[26]	-1310.75	80.5	388	SEG[102]	-2951	238								
324	COM[25]	-1335.25	225.5	389	SEG[100]	-2975.5	98								
325	COM[24]	-1359.75	80.5	390	SEG[98]	-3000	238								
326	COM[23]	-1384.25	225.5	391	SEG[96]	-3024.5	98								
327	COM[22]	-1408.75	80.5	392	SEG[94]	-3049	238								
328	COM[21]	-1433.25	225.5	393	SEG[92]	-3073.5	98								
329	COM[20]	-1457.75	80.5	394	SEG[90]	-3098	238								
330	COM[19]	-1482.25	225.5	395	SEG[88]	-3122.5	98								
331	COM[18]	-1506.75	80.5	396	SEG[86]	-3147	238								
332	COM[17]	-1531.25	225.5	397	SEG[84]	-3171.5	98								
333	COM[16]	-1555.75	80.5	398	SEG[82]	-3196	238								
334	COM[15]	-1580.25	225.5	399	SEG[80]	-3220.5	98								
335	COM[14]	-1604.75	80.5	400	SEG[78]	-3245	238								
336	COM[13]	-1629.25	225.5	401	SEG[76]	-3269.5	98								
337	COM[12]	-1653.75	80.5	402	SEG[74]	-3294	238								
338	COM[11]	-1678.25	225.5	403	SEG[72]	-3318.5	98								
339	COM[10]	-1702.75	80.5	404	SEG[70]	-3343	238								
340	COM[9]	-1727.25	225.5	405	SEG[68]	-3367.5	98								
341	COM[8]	-1751.75	80.5	406	SEG[66]	-3392	238								
342	COM[7]	-1776.25	225.5	407	SEG[64]	-3416.5	98								
343	COM[6]	-1800.75	80.5	408	SEG[62]	-3441	238								
344	COM[5]	-1825.25	225.5	409	SEG[60]	-3465.5	98								
345	COM[4]	-1849.75	80.5	410	SEG[58]	-3490	238								

6. Function Description

6.1. Microprocessor Interface Selection

The 8080-Parallel Interface, 6800-Parallel Interface, Serial Interface (SPI) can be selected by different selections of IM0~2 as shown in Table 1.

Table 1

Interface	Config			Data signal								Control signal				
	IM0	IM1	IM2	D7	D6	D5	D4	D3	D2	D1	D0	E/RDB	WRB	CSB	A0	RESB
6800	1	0	0	D7	D6	D5	D4	D3	D2	D1	D0	E	R/$\overline{W}$	$\overline{CS}$	A0	$\overline{RES}$
8080	0	1	1	D7	D6	D5	D4	D3	D2	D1	D0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	A0	$\overline{RES}$
4-Wire SPI	0	0	0	Hz (Note1)					SO (Note2)	SI/SO (Note2)	SCL	Pull Low		$\overline{CS}$	A0	$\overline{RES}$
3-Wire SPI	0	0	1	Hz (Note1)					SO (Note2)	SI/SO (Note2)	SCL	Pull Low		$\overline{CS}$	Pull Low	$\overline{RES}$
I2C	0	1	0	Hz (Note1)						SDA	SCL	Pull Low		Pull Low	SA0	$\overline{RES}$

Note1: When Serial Interface (SPI) or I^2C Interface is selected, D7~D2 is Hz. D7~D2 is recommended to connect the VDD or GND. It is also allowed to leave D7~D2 unconnected.

Note2: When Serial Interface (SPI) is selected, data output to data pin D1 or D2 in read cmd or ram.

92h = 0x00 (or not 0x69), SPI data output to data pin D1. (default)

92h = 0x69, SPI data output to data pin D2.

Please Refer to CH1120_App.Note document.

6.2. 6800-series Parallel Interface

The parallel interface consists of 8 bi-directional data pads (D7-D0), R/$\overline{W}$, E, A0 and $\overline{CS}$ .It includes 2 forms.

Form 1: A falling edge of E input serve as READ latch signal while $\overline{CS}$ is kept low and R/$\overline{W}$ is kept high. A falling edge of E input serve as WRITE latch signal while $\overline{CS}$ is kept low and R/$\overline{W}$ is kept low. This is shown in Table.2 below.

Table 2 (Form 1)

Function	$\overline{CS}$	A0	R/$\overline{W}$	E
Write command	L	L	L	↓
Read status	L	L	H	↓
Write data	L	H	L	↓
Read data	L	H	H	↓

Note:

1. ' ↓ 'stands for falling edge of signal.
2. ' H 'stands for high in signal, ' L ' stands for low in signal.

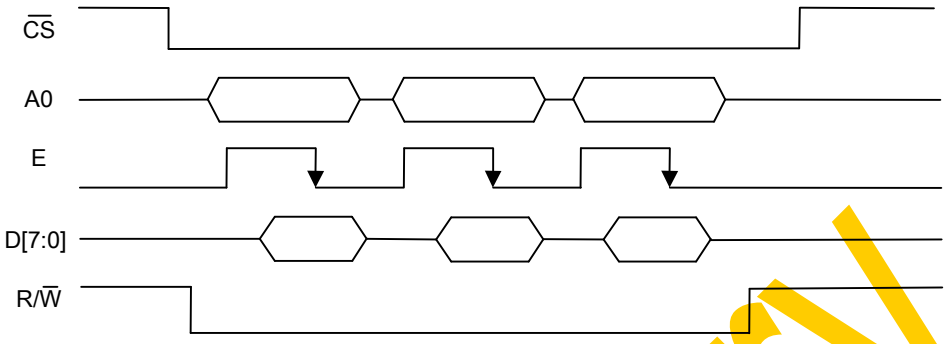


Figure 1 Example of write procedure in 6800 parallel interface form 1

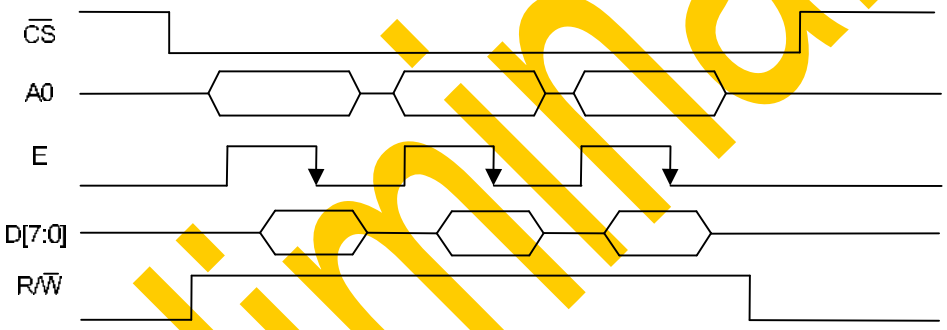


Figure 2 Example of read procedure in 6800 parallel interface form 1

Form 2: A rising edge of $\overline{CS}$ input serve as READ latch signal while E is kept high and $R/\overline{W}$ is kept high. A rising edge of $\overline{CS}$ input serve as WRITE latch signal while E is kept high and $R/\overline{W}$ is kept low. A low in A0 indicates COMMAND read/write and high in A0 indicates DATA read/write. This is shown in Table.3 below.

Table 3 (6800 Form 2)

Function	$\overline{CS}$	A0	$R/\overline{W}$	E
Write command	↑	L	L	H
Read status	↑	L	H	H
Write data	↑	H	L	H
Read data	↑	H	H	H

Note:

1. ' ↑ 'stands for rising edge of signal.
2. ' H 'stands for high in signal, ' L ' stands for low in signal.

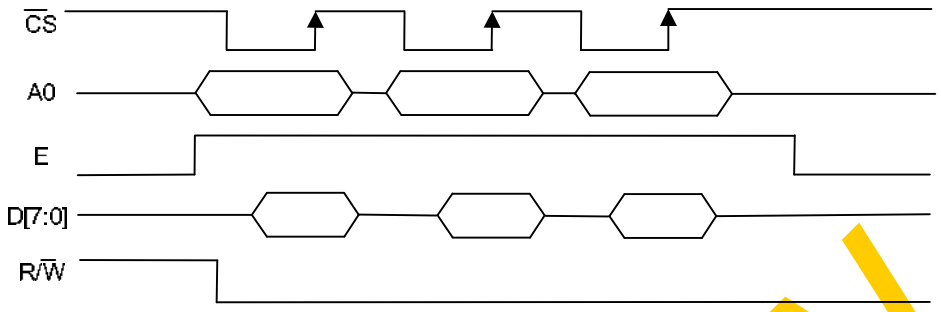


Figure 3 Example of write procedure in 6800 parallel interface form 2

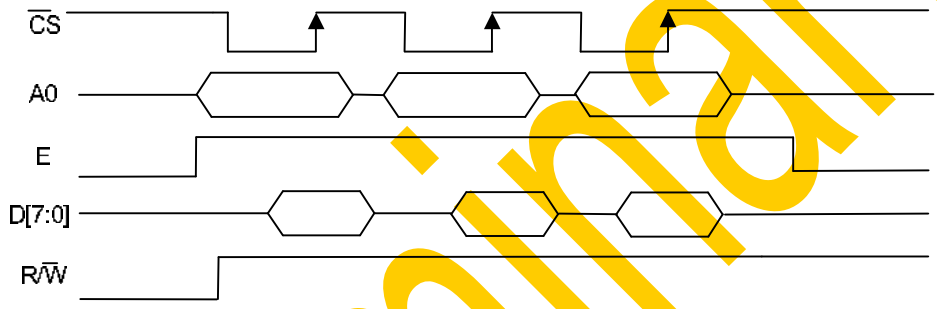


Figure 4 Example of read procedure in 6800 parallel interface form 2

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing are internally performed, which require the insertion of a dummy read before the first actual display data read. This is shown in Figure. 5 below.

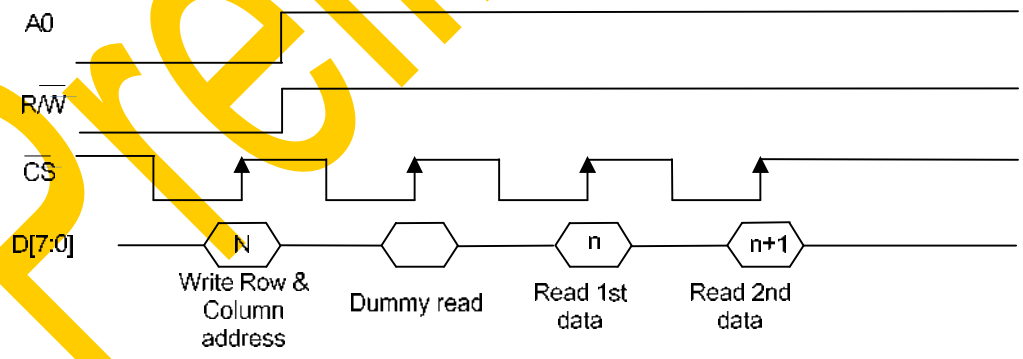


Figure 5 Read RAM data process–insertion of dummy read

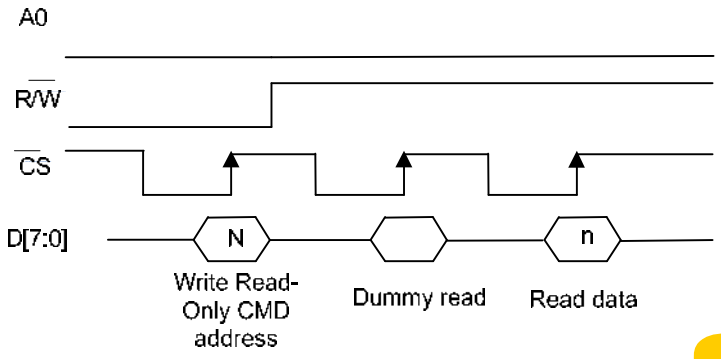


Figure6 Read Read-Only CMD process–insertion of dummy read

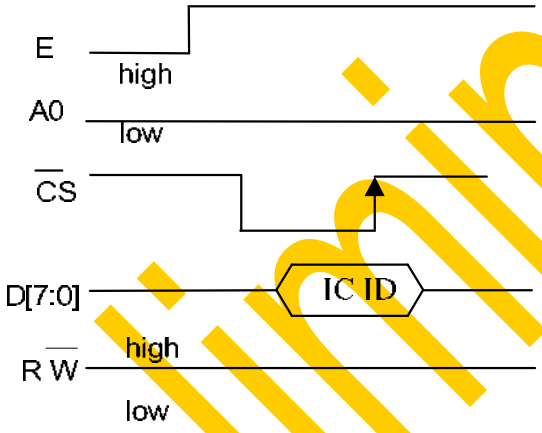


Figure 7 Read status process–no dummy read

Note. When finish writing or reading, CS must keep high in form1 and E must keep low in form2.

6.3. 8080-series Parallel Interface

The parallel interface consists of 8 bi-directional data pads (D7-D0), $\overline{WR}$, $\overline{RD}$, A0 and $\overline{CS}$. It includes 2 forms.

Form 1: A rising edge of $\overline{RD}$ input serve as data READ latch signal while $\overline{CS}$ is kept low. A rising edge of $\overline{WR}$ input serve as data/command Write latch signal while $\overline{CS}$ is kept low. A low in A0 indicates COMMAND read/write and high in A0 indicates DATA read/write. This is shown in Table.4 below.

Table 4 (8080 Form1)

Function	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$
Write command	L	L	H	↑
Read status	L	L	↑	H
Write data	L	H	H	↑
Read data	L	H	↑	H

Note:

1. ' ↑ 'stands for rising edge of signal.
2. ' H 'stands for high in signal, ' L ' stands for low in signal.

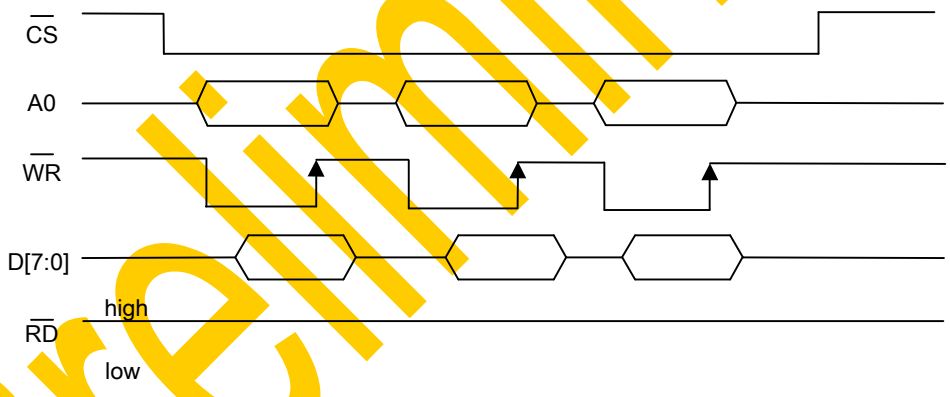


Figure 8 Example of write procedure in 8080 parallel interface form 1

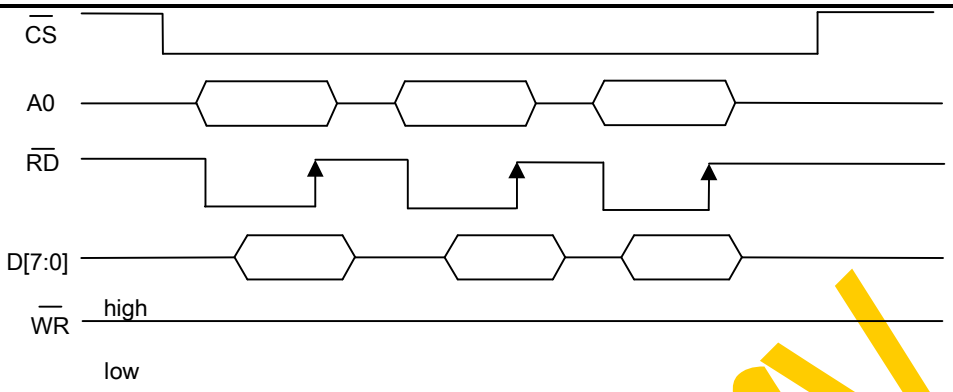


Figure 9 Example of read procedure in 8080 parallel interface form 1

Form 2: A rising edge of $\overline{CS}$ input serve as data READ latch signal while $\overline{RD}$ is kept low. A rising edge of $\overline{CS}$ input serve as data Write latch signal while $\overline{WR}$ is kept low. A low in A0 indicates COMMAND read/write and high in A0 indicates DATA read/write. This is shown in Table.5 below.

Table 5 (8080 Form2)

Function	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$
Write command	↑	L	H	L
Read status	↑	L	L	H
Write data	↑	H	H	L
Read data	↑	H	L	H

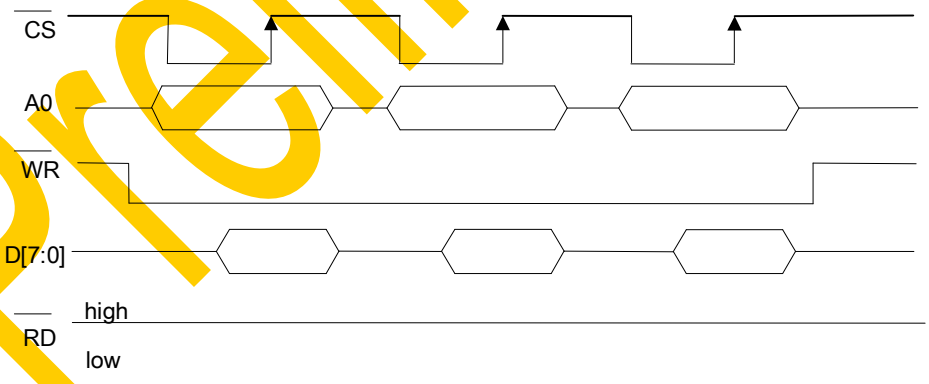


Figure 10 Example of write procedure in 8080 parallel interface form 2

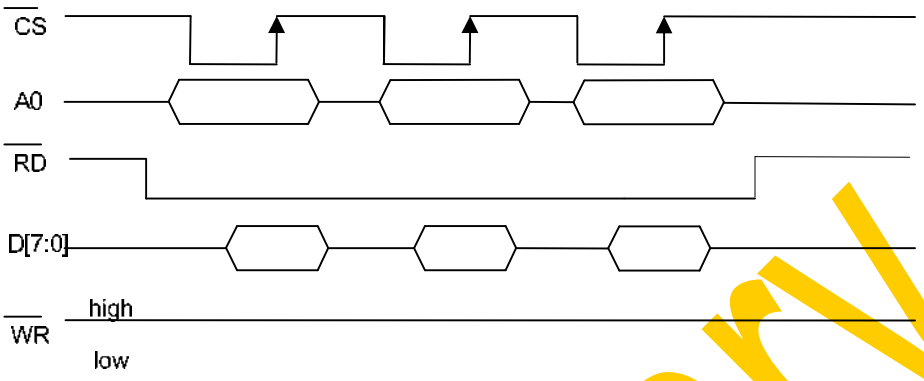


Figure 11 Example of read procedure in 8080 parallel interface form 2

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing are internally performed, which require the insertion of a dummy read before the first actual display data read. This is shown in Figure. 10 below.

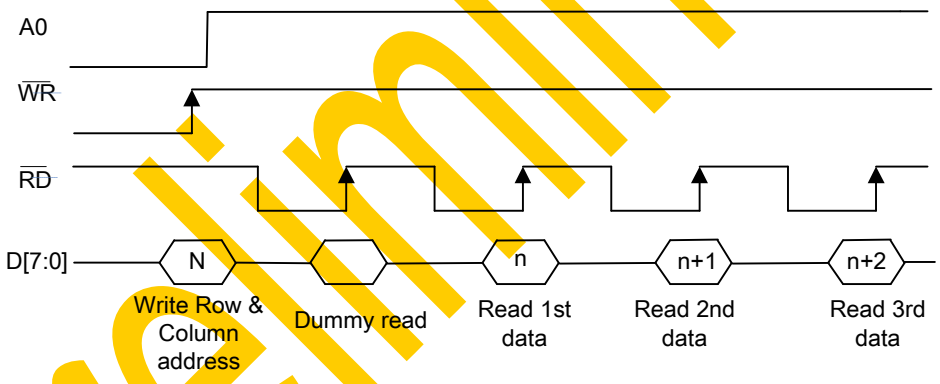


Figure 12 Read RAM data process–insertion of dummy read

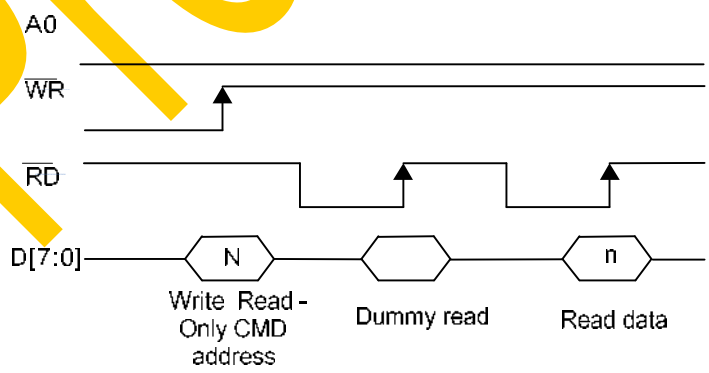


Figure 13 Read Read-Only CMD process–insertion of dummy read

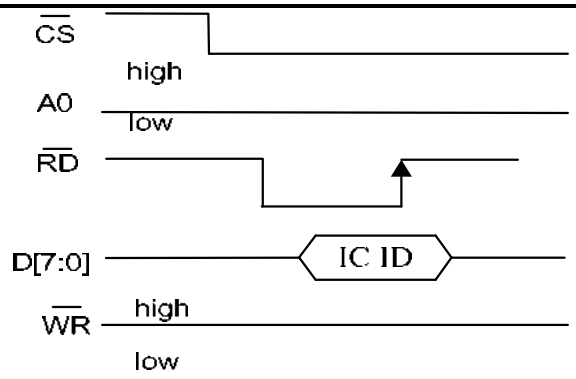


Figure 14 Read status process–no dummy read

Note. When finish writing or reading, CS must keep high in form1 and WR/RD must keep high in form2.

6.4. 4 Wire Serial Interface (4-wire SPI)

The serial interface consists of serial clock SCL, serial data SI, A0 and $\overline{CS}$. SI is shifted into an 8-bit shift register on every rising edge of SCL in the order of D7, D6 … and D0. A0 is sampled on every eighth clock and the data byte in the shift register is written to the display data RAM (A0=1) or command register (A0=0) in the same clock. See figure 11

Table 6

IM0	IM1	IM2	Type	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	D0	D1	D2	D2 to D7
0	0	0	4-wire SPI	$\overline{CS}$	A0	-	-	SCL	SI/SO	SO	(Hi-z)

Note: "-" pin must always be HIGH or LOW. D7~D2 is recommended to connect the VDD or GND. It's also allowed to leave D7~D2 unconnected.

The serial interface is initialized when $\overline{CS}$ is high. In this state, SCL clock pulse or SDI data have no effect. A falling edge on $\overline{CS}$ enables the serial interface and indicates the start of data transmission. The SPI is also able to work properly when the $\overline{CS}$ always keep low, but it is not recommended. When finish writing or reading, CS must keep high.

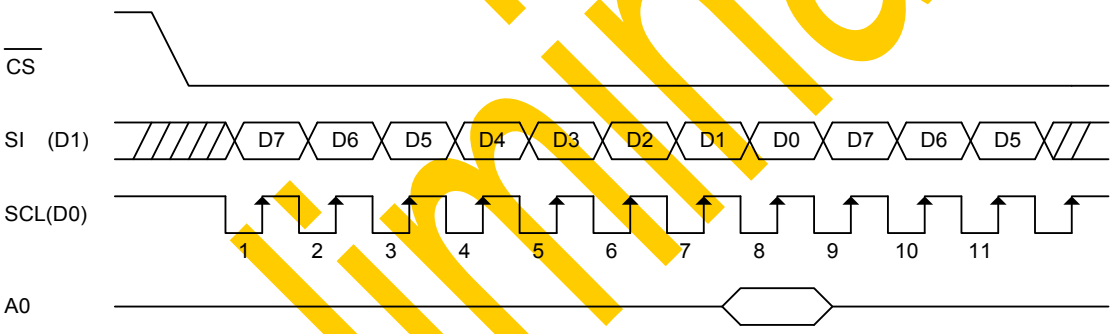
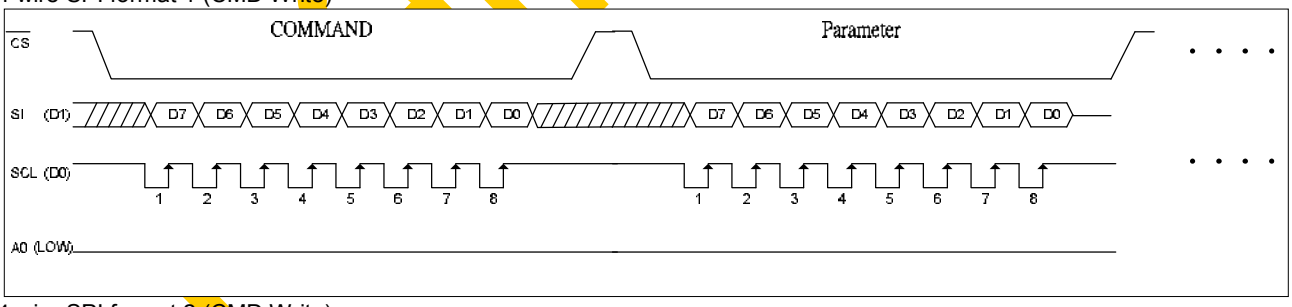
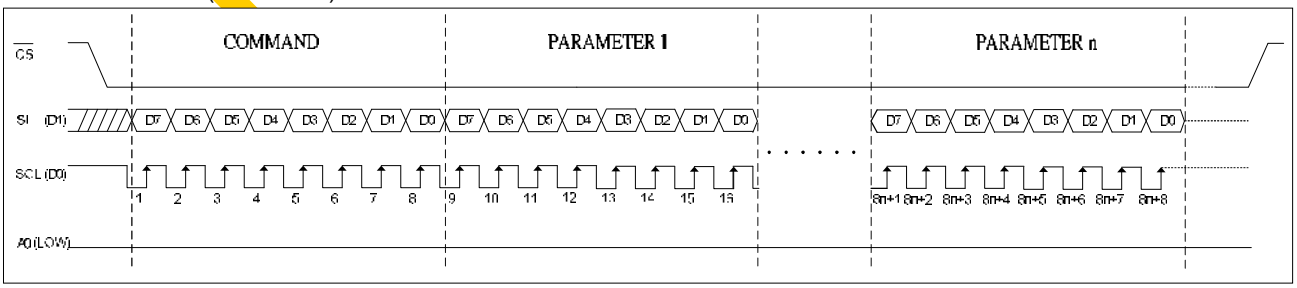


Figure 11 4-wire SPI data transfer

4 wire SPI format 1 (CMD Write)

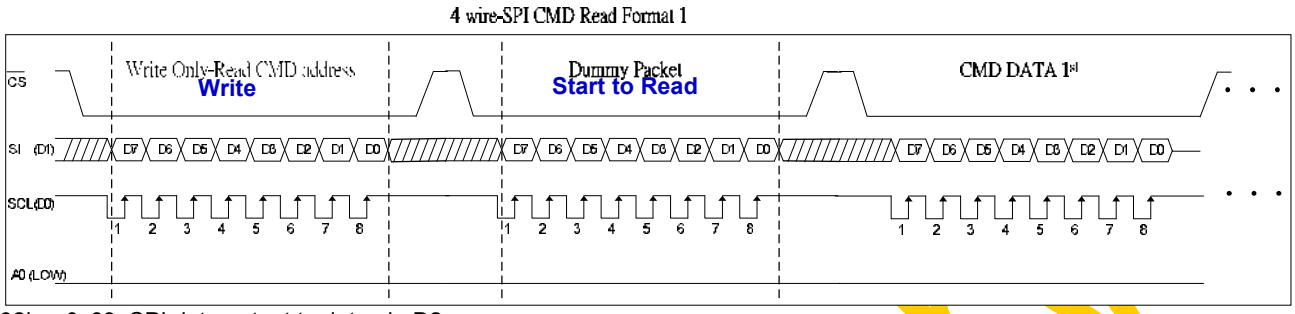


4 wire SPI format 2 (CMD Write)

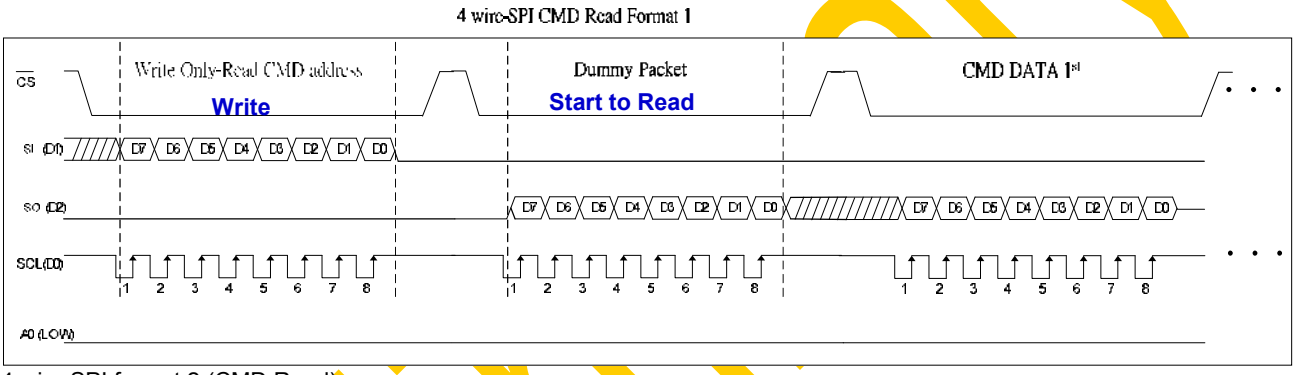


4 wire SPI format 1 (CMD Read)

92h = 0x00 (or not 0x69) , SPI data output to data pin D1. (default)

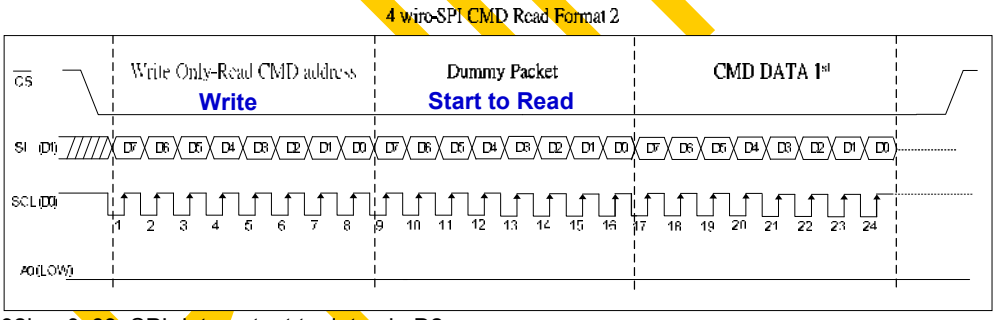


92h = 0x69, SPI data output to data pin D2.



4 wire SPI format 2 (CMD Read)

92h = 0x00 (or not 0x69) , SPI data output to data pin D1. (default)



92h = 0x69, SPI data output to data pin D2.

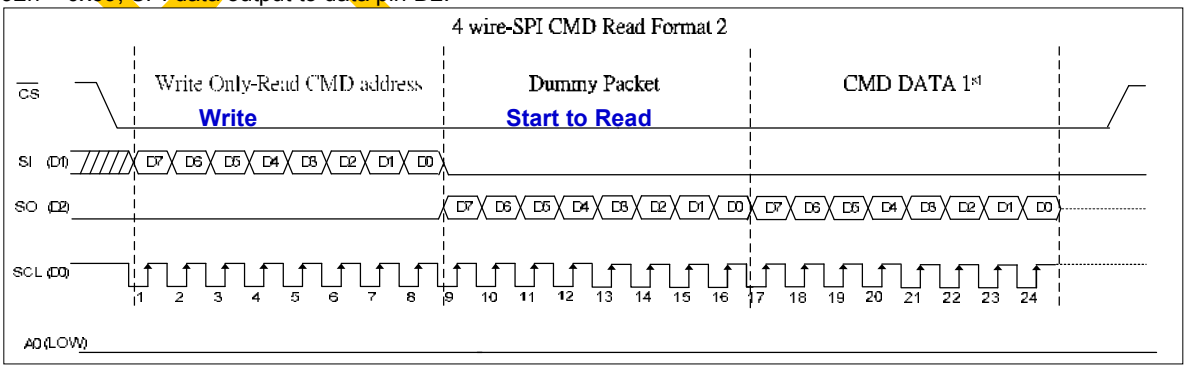
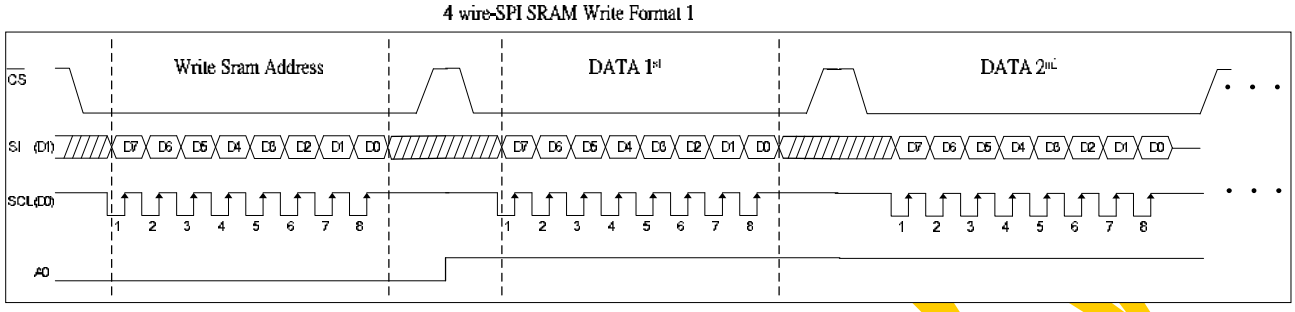


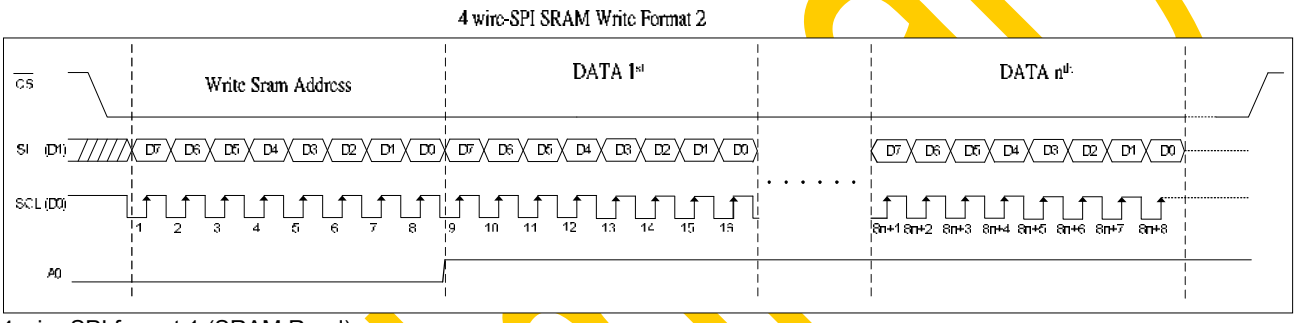
Figure 12 4-wire SPI Read Only-Read CMD data

When the chip is not active, the shift registers and the counter are reset to their initial statuses. Read is only for Only-Read CMD. When finish read cmd , CSB signal must be pull high. Caution is required on the SCL signal when it comes to line-end reflections and external noise. We recommend the operation be rechecked on the actual equipment.

4 wire SPI format 1 (SRAM Write)

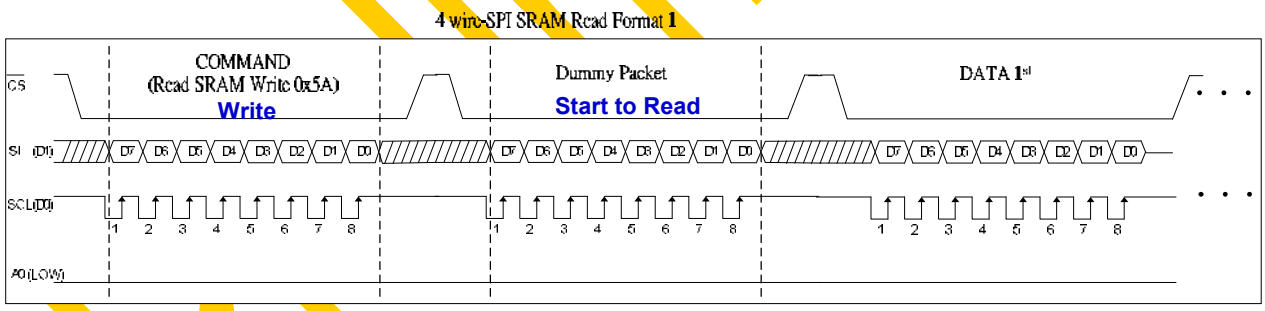


4 wire SPI format 2 (SRAM Write)

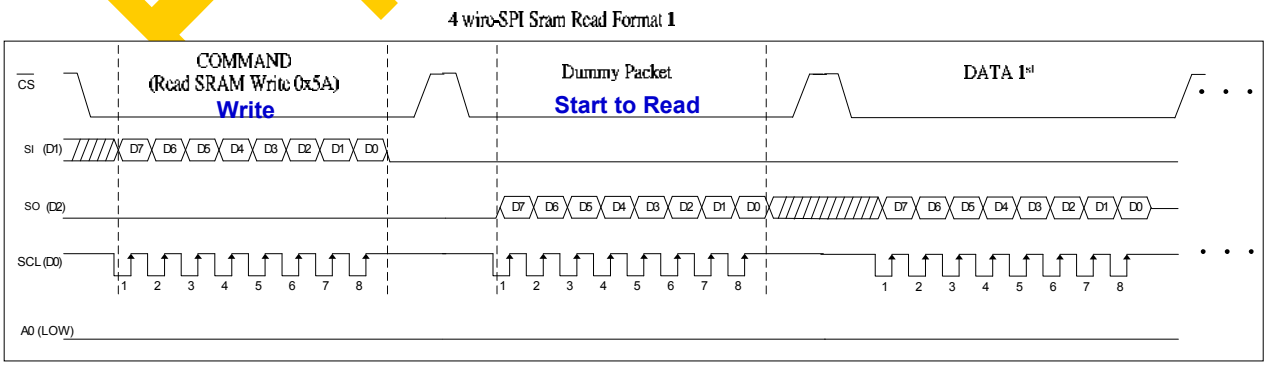


4 wire SPI format 1 (SRAM Read)

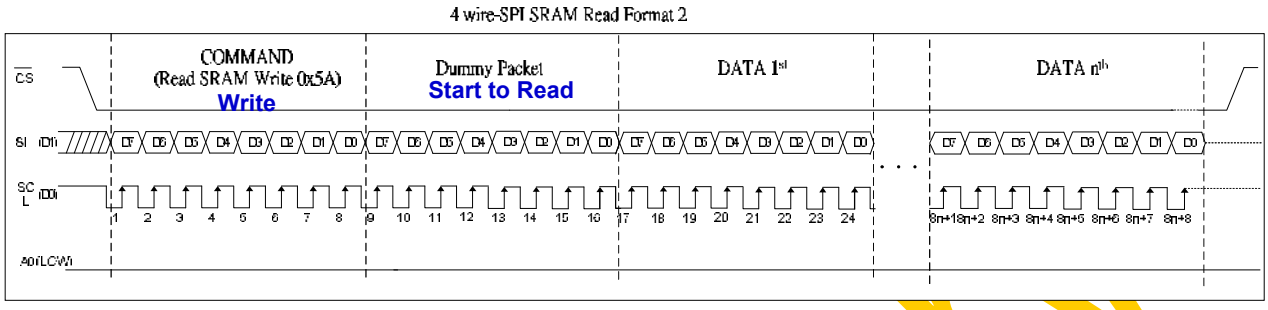
92h = 0x00 (or not 0x69) , SPI data output to data pin D1. (default)



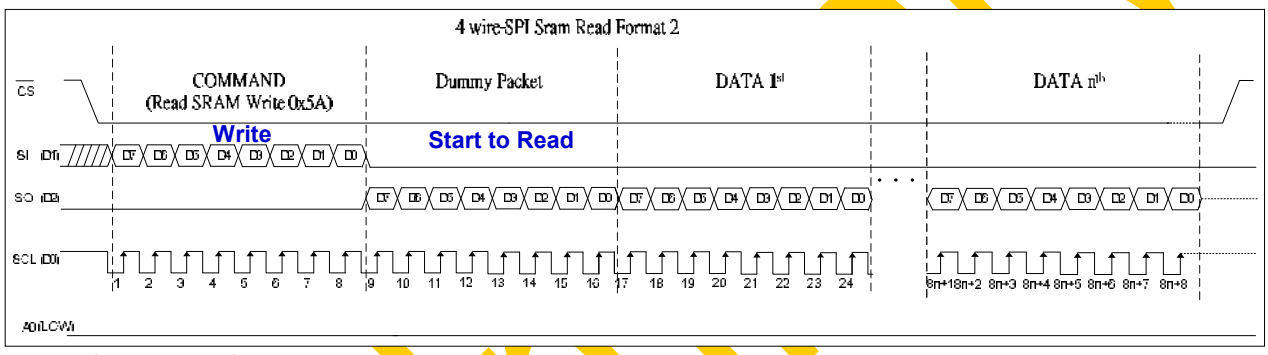
92h = 0x69, SPI data output to data pin D2.



4 wire SPI format 2 (SRAM Read)
92h = 0x00 (or not 0x69) , SPI data output to data pin D1.
(default)



92h = 0x69, SPI data output to data pin D2.



Note1：SRAM Read Command Write 5Ah
Note2： When using SPI read SRAM：
① More than two SRAM addresses must be set；
② The SRAM data in the set address range must be read all at once.

6.5. 3 Wire Serial Interface (3-wire SPI)

The 3 wire serial interface consists of serial clock SCL, serial data SI, and $\overline{CS}$. SI is shifted into a 9-bit shift register on every rising edge of SCL in the order of $D/\overline{C}$, D7, D6 … D0. The $D/\overline{C}$ bit (first of the 9 bit) will determine the transferred data is written to the display data RAM ($D/\overline{C}$=1) or command register ($D/\overline{C}$=0). See figure 12.

Table 7

IM0	IM1	IM2	Type	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	D0	D1	D2	D2 to D17
0	0	1	3-wire SPI	$\overline{CS}$	Pull Low	-	-	SCL	SI/SO	SO	(Hi-z)

Note: "-" pin must always be HIGH or LOW. D7~ D2 is recommended to connect the VDD or GND. It is also allowed to leave D7~ D2 unconnected.

The serial interface is initialized when $\overline{CS}$ is high. In this state, SCL clock pulse or SDI data have no effect. A falling edge on $\overline{CS}$ enables the serial interface and indicates the start of data transmission. The SPI is also able to work properly when the $\overline{CS}$ always keep low, but it is not recommended. When finish writing or reading, CS must keep high.

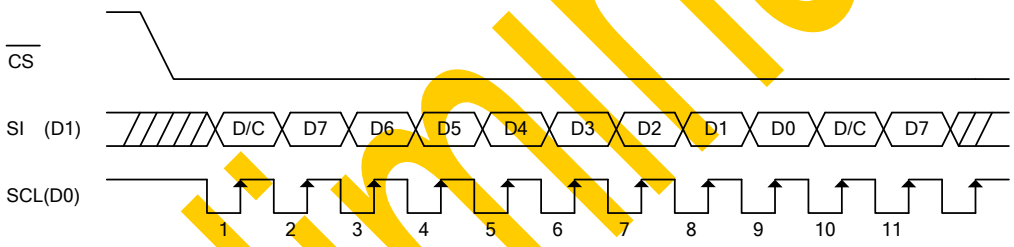
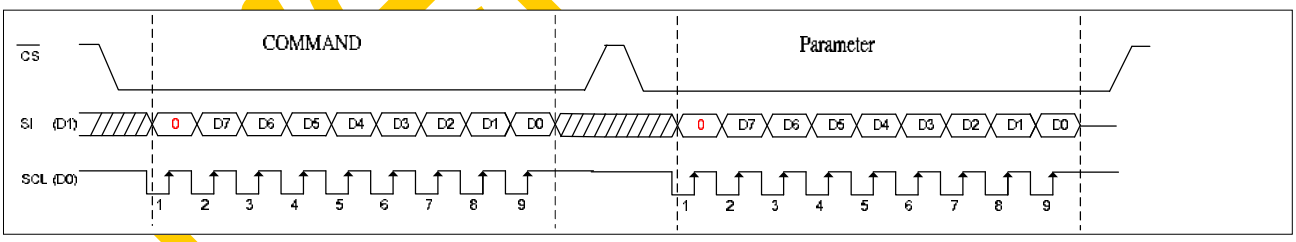
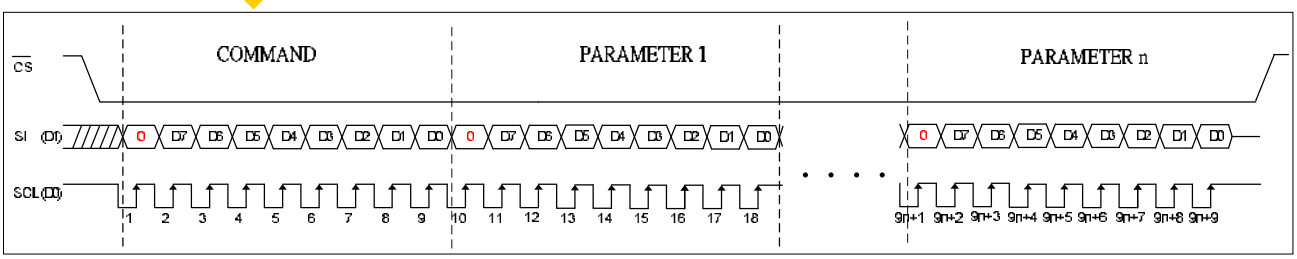


Figure12 3-wire SPI data transfer

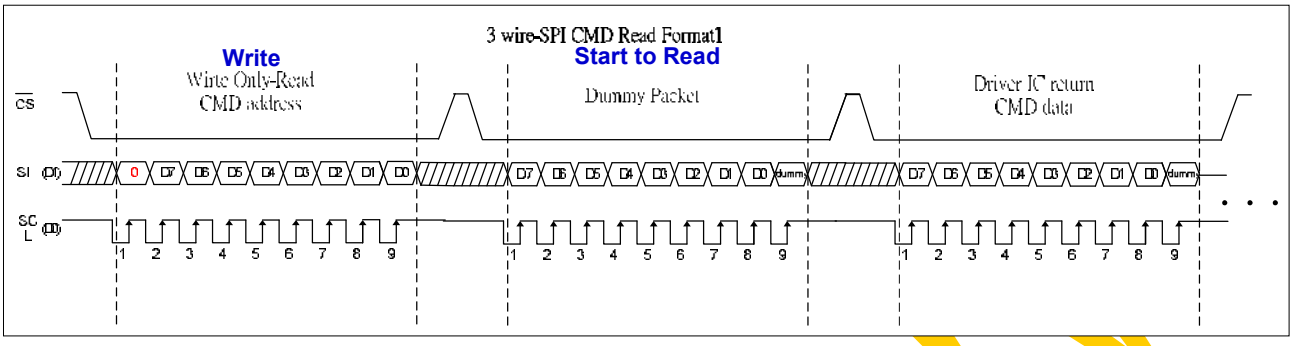
3 wire SPI format 1 (CMD Write)



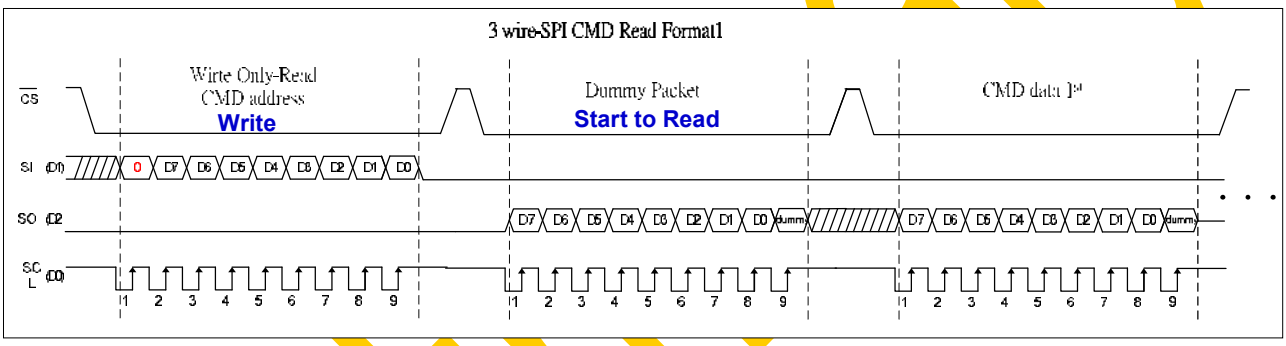
3 wire SPI format 2 (CMD Write)



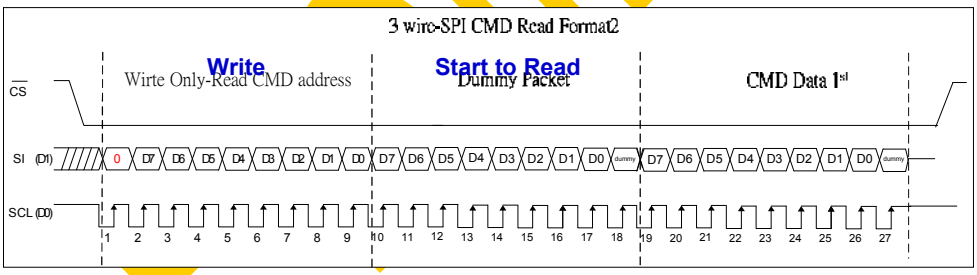
3 wire SPI format 1 (CMD Read)
92h = 0x00 (or not 0x69) , SPI data output to data pin D1.
(default)



92h = 0x69, SPI data output to data pin D2.



3 wire SPI format 2 (CMD Read)
92h = 0x00 (or not 0x69) , SPI data output to data pin D1.
(default)



92h = 0x69, SPI data output to data pin D2.

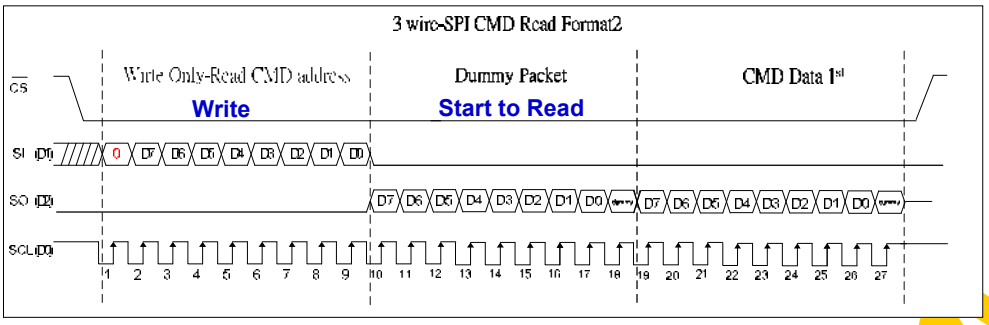
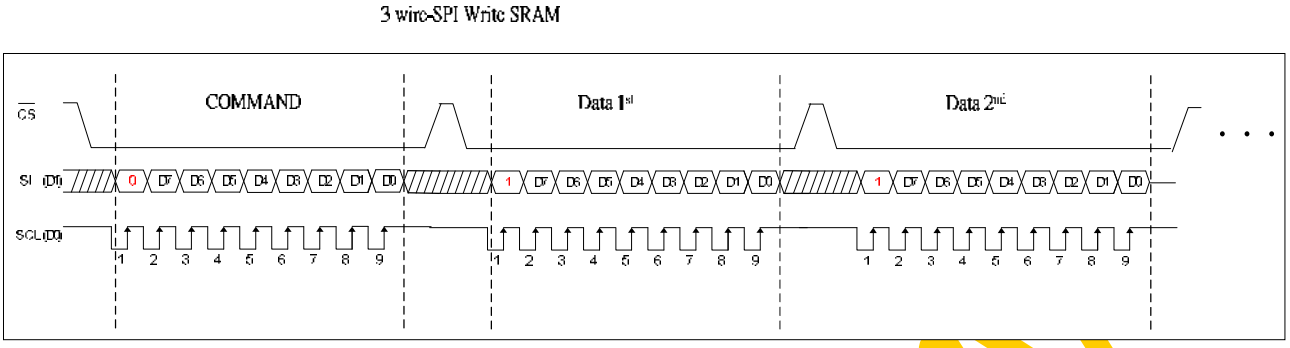


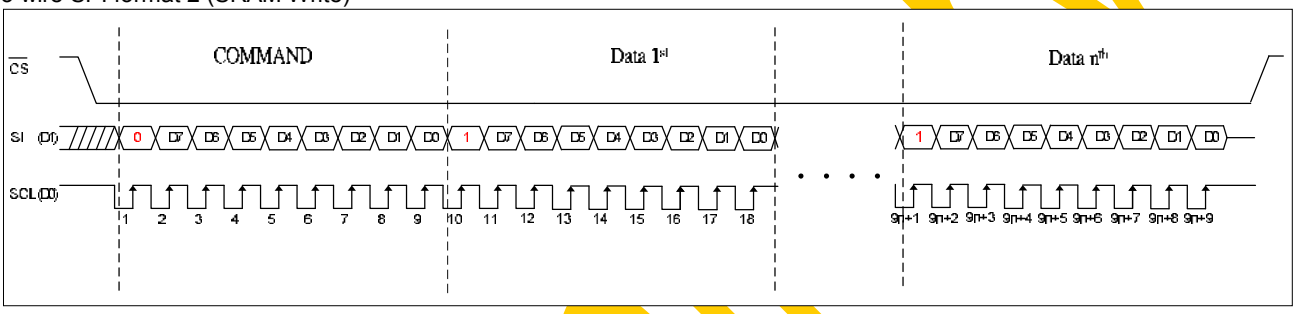
Figure13 3-wire SPI Read Only-Read CMD data

When the chip is not active, the shift registers and the counter are reset to their initial statuses. Read is only for Only-Read CMD. When finish read cmd , CSB signal must be pull high. Caution is required on the SCL signal when it comes to line-end reflections and external noise. We recommend the operation be rechecked on the actual equipment.

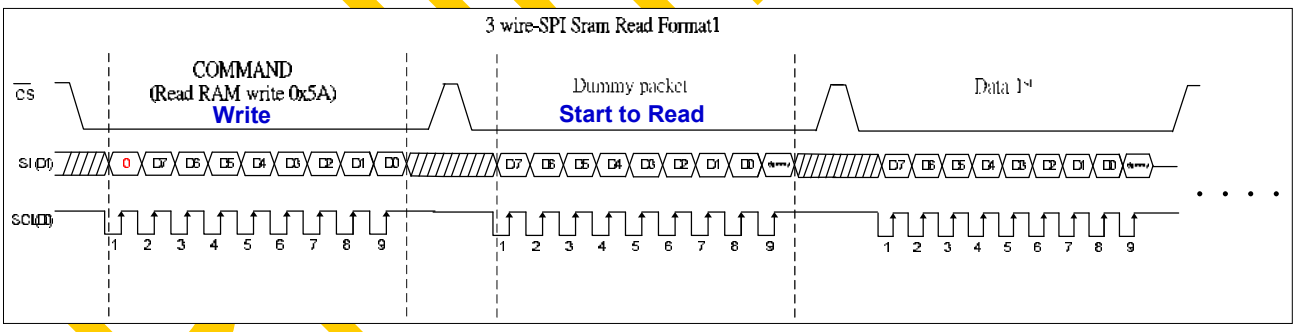
3 wire SPI format 1 (SRAM Write)



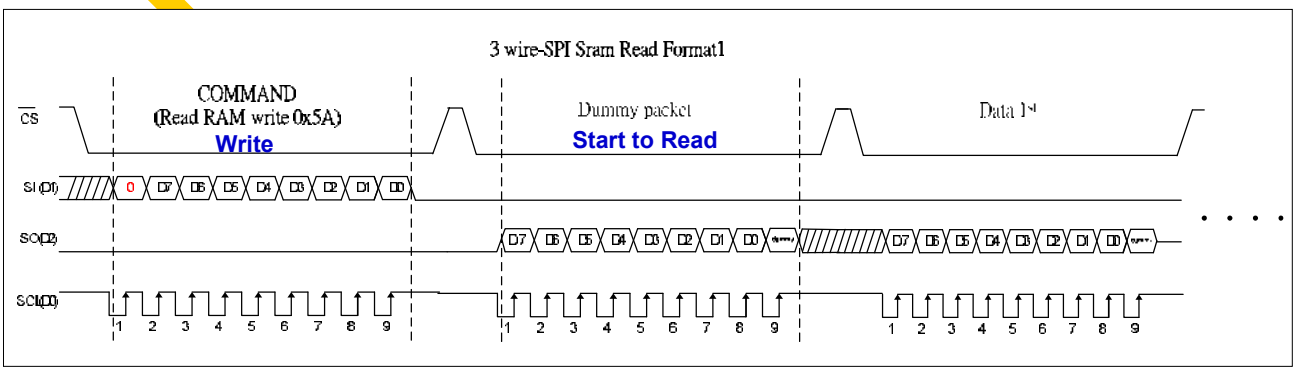
3 wire SPI format 2 (SRAM Write)



3 wire SPI format 1 (SRAM Read)
92h = 0x00 (or not 0x69) , SPI data output to data pin D1. (default)

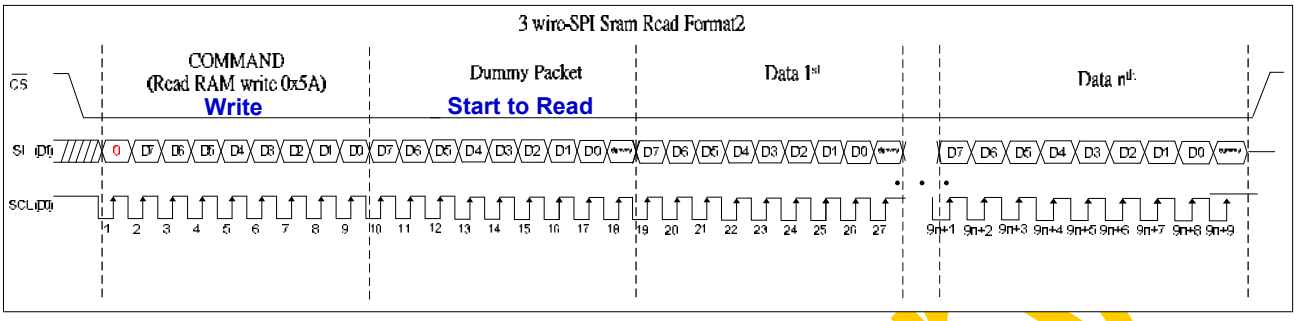


92h = 0x69, SPI data output to data pin D2.

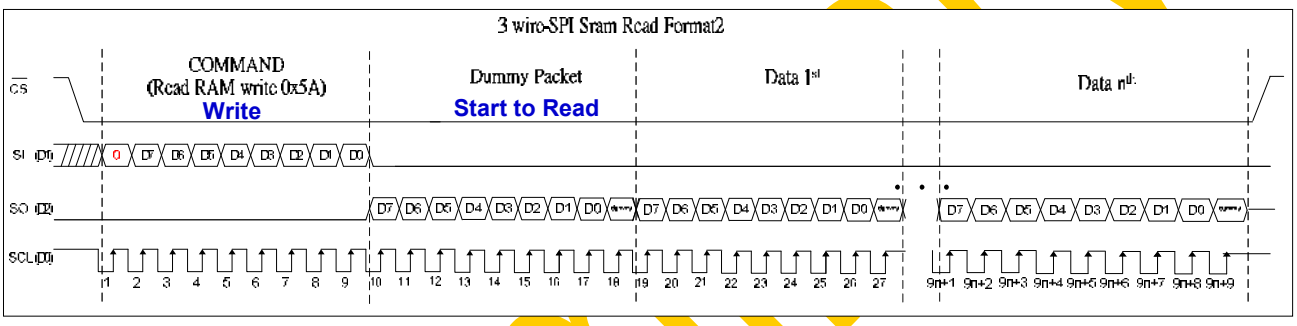


3 wire SPI format 2 (SRAM Read)

92h = 0x00 (or not 0x69) , SPI data output to data pin D1. (default)



92h = 0x69, SPI data output to data pin D2.



Note1：. SRAM Read Command Write 5Ah

Note2： When using SPI read SRAM：

① More than two SRAM addresses must be set；

② The SRAM data in the set address range must be read all at once.

6.6. I²C-bus Interface

The CH1120 can transfer data via a standard I²C-bus and has slave mode only in communication. The command or RAM data can be written into the chip and the status can be read out of the chip.

Table 8

IM0	IM1	IM2	Type	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	D0	D1	D2 to D17
0	1	0	I²C Interface	$\overline{CS}$	SA0	-	-	SCL	SI	(Hi-z)

Note: "-" pin must always be HIGH or LOW. D7~ D2 is recommended to connect the VDD or GND. It is also allowed to leave D7~ D2 unconnected.

$\overline{CS}$ Signal could always pull low in I²C-bus application.

6.6.1. Characteristics of the I2C-bus

The I²C-bus is for bi-directional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

Note: The positive supply of pull-up resistor must equal to the value of VDD.

6.6.2. Bit Transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.

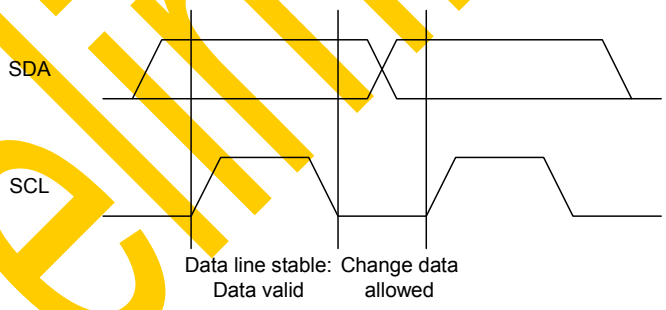


Figure 13 Bit Transfer

6.6.3. Start and Stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P).

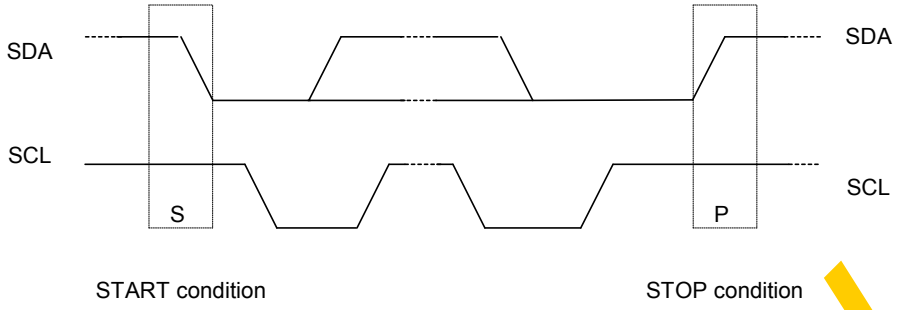


Figure 14 Start and Stop conditions

6.6.4. System configuration

- Transmitter: The device that sends the data to the bus.
- Receiver: The device that receives the data from the bus.
- Master: The device that initiates a transfer generates clock signals and terminates a transfer.
- Slave: The device addressed by a master.
- Multi-Master: More than one master can attempt to control the bus at the same time without corrupting the message
- Arbitration: Procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted.
- Synchronization: Procedure to synchronize the clock signals of two or more devices.

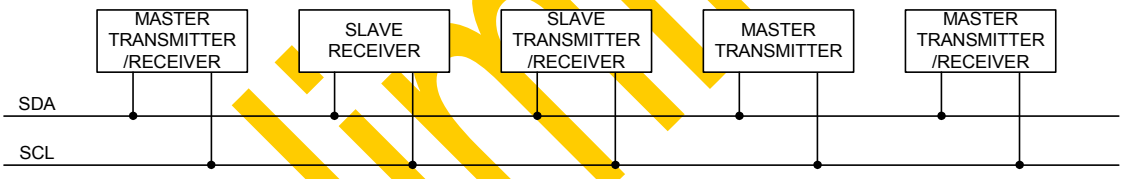


Figure 15 System configuration

6.6.5. Acknowledge

Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

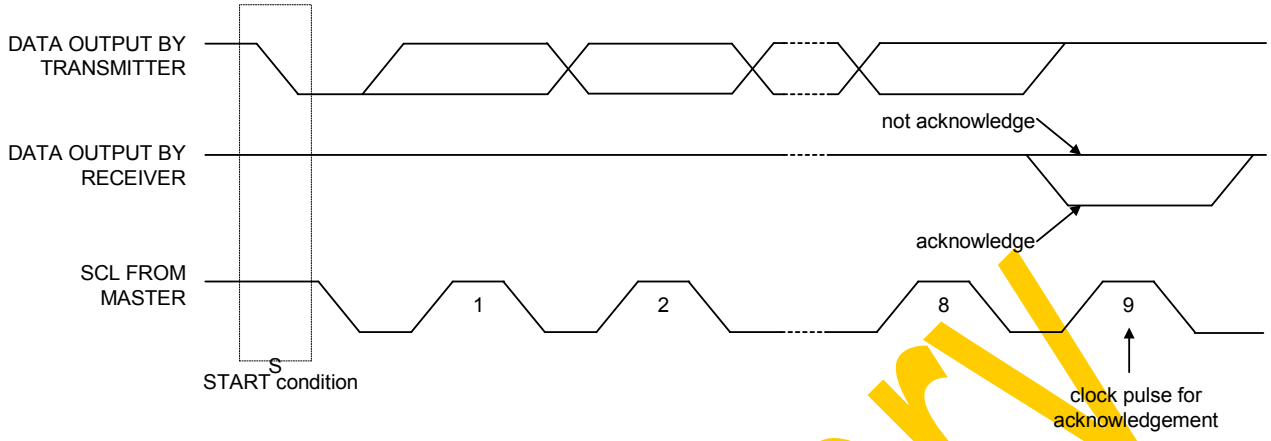


Figure 16 Acknowledge

6.6.6. Protocol

The CH1120 supports both read and write access. The $R/\overline{W}$ bit is part of the slave address. Before any data is transmitted on the I²C-bus, the device that should respond is addressed first. Two 7-bit slave addresses (0111100 and 0111101) are reserved for the CH1120. The least significant bit of the slave address is set by connecting the input SA0 to either logic 0(GND) or 1 (VDD). The I²C-bus protocol is illustrated in Fig.14. The sequence is initiated with a START condition (S) from the I²C-bus master that is followed by the slave address. All slaves with the corresponding address acknowledge in parallel, all the others will ignore the I²C-bus transfer. After acknowledgement, one or more command words follow which define the status of the addressed slaves. A command word consists of a control byte, which defines Co and $D/\overline{C}$ (note1), plus a data byte (see Fig.19). The last control byte is tagged with a cleared most significant bit, the continuation bit Co. After a control byte with a cleared Co-bit, only data bytes will follow. The state of the $D/\overline{C}$-bit defines whether the data-byte is interpreted as a command or as RAM-data. The control and data bytes are also acknowledged by all addressed slaves on the bus. After the last control byte, depending on the $D/\overline{C}$ bit setting, either a series of display data bytes or command data bytes may follow. If the $D/\overline{C}$ bit was set to '1', these display bytes are stored in the display RAM at the address specified by the data pointer. The data pointer is automatically updated and the data is directed to the intended CH1120 device. If the $D/\overline{C}$ bit of the last control byte was set to '0', these command bytes will be decoded and the setting of the device will be changed according to the received commands. The acknowledgement after each byte is made only by the addressed slave. At the end of the transmission the I²C-bus master issues a stop condition (P). If the $R/\overline{W}$ bit is set to one in the slave-address, the chip will output data immediately after the slave-address according to the $D/\overline{C}$ bit, which was sent during the last write access. If no acknowledge is generated by the master after a byte, the driver stops transferring data to the master.

Whether the dummy packet needed or not in the read protocol of all interface as below:

I/F	Read Status	Only-Read CMD	Read Ram data
I2C	No dummy packet	No dummy packet	Do not support

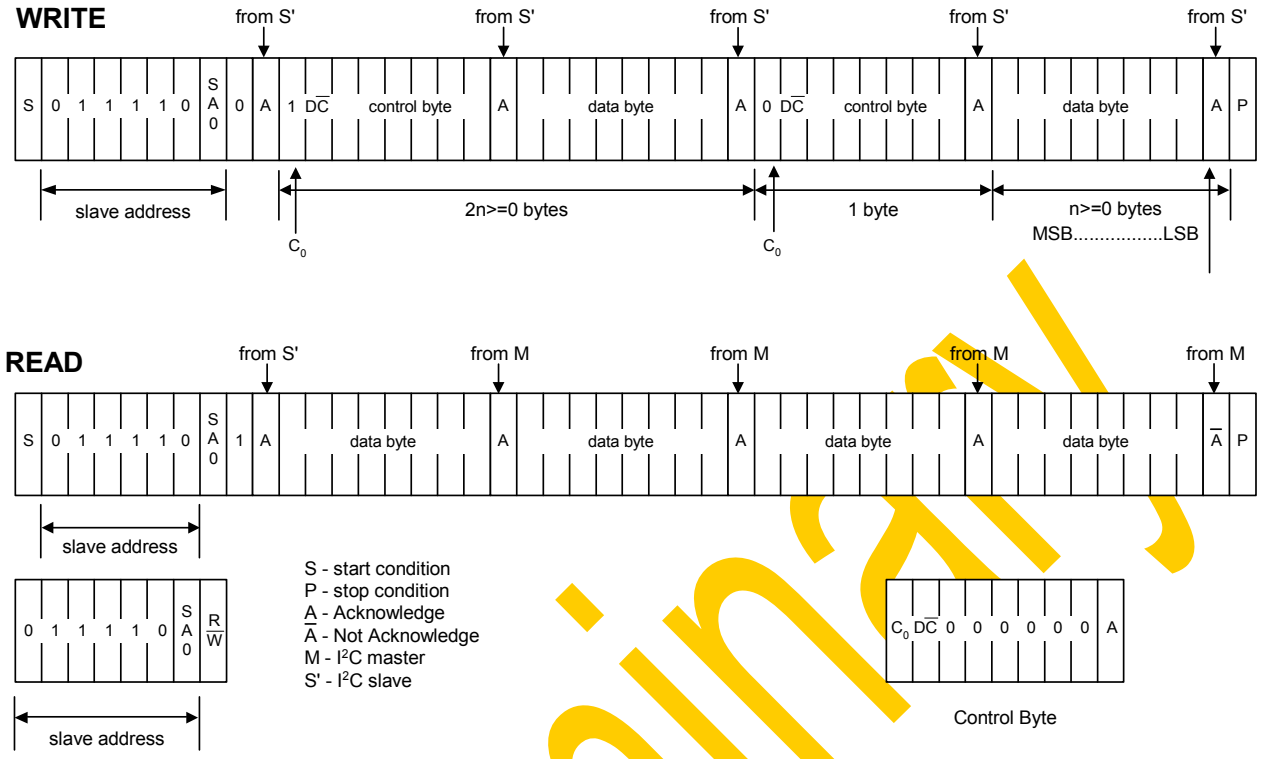


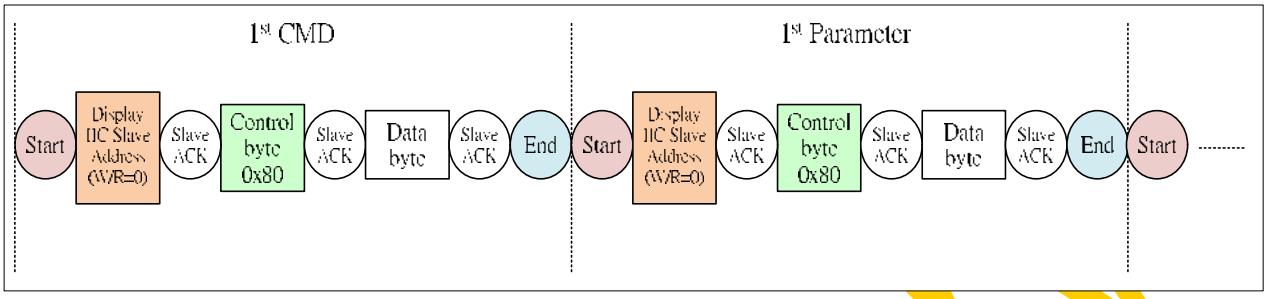
Figure 17 I²C Protocol

Note1:

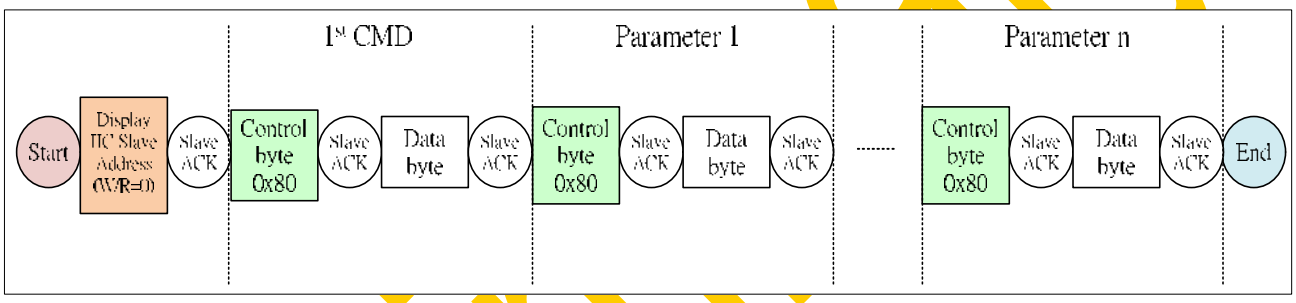
1. Co= "0" : The last control byte , only data bytes to follow,
   Co= "1" : Next two bytes are a data byte and another control byte;
2. D/C = "0" : The data byte is for command operation,
   D/C = "1" : The data byte is for RAM operation.

Support write format as below:

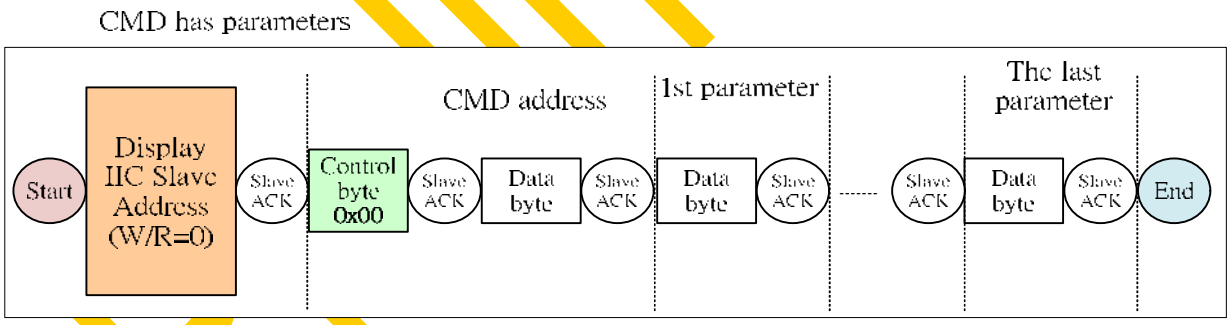
Write CMD format 1



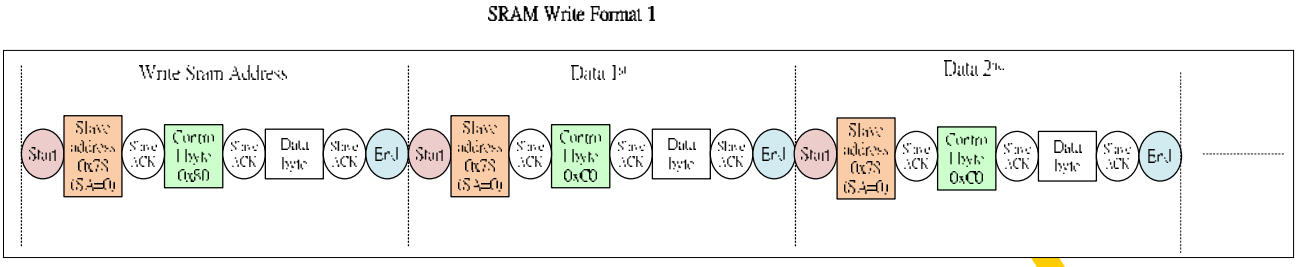
Write CMD format 2



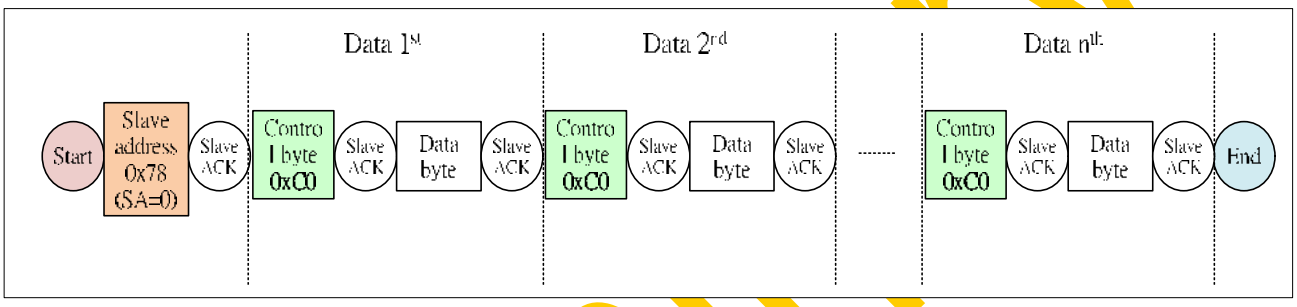
Write CMD format 3



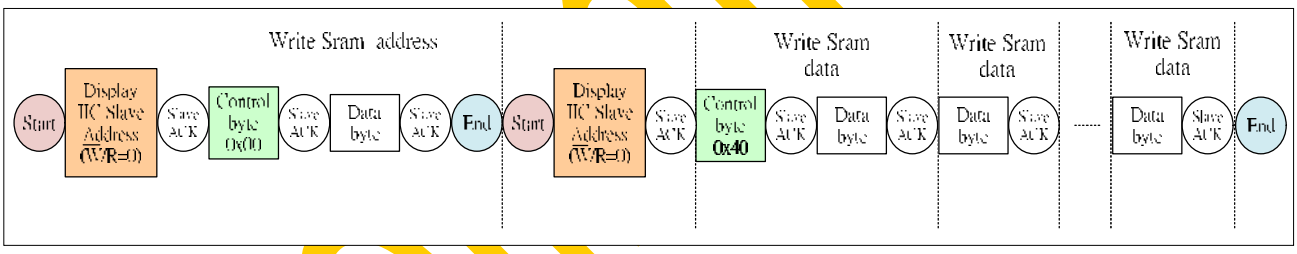
Write SRAM format 1



Write SRAM format 2

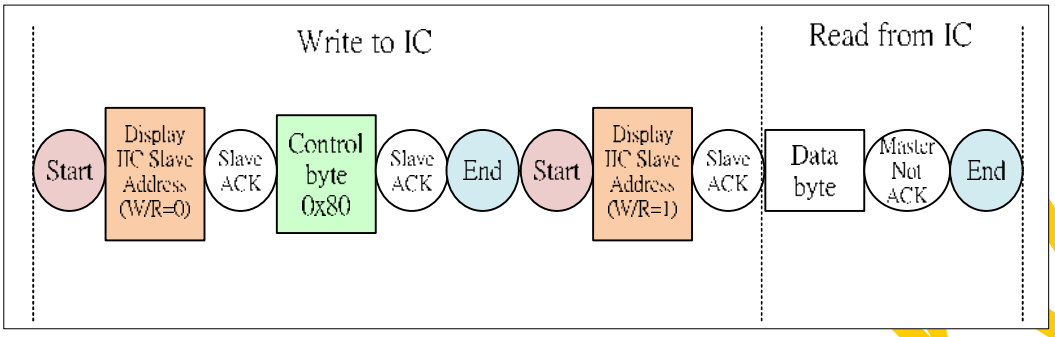


Write SRAM format 3

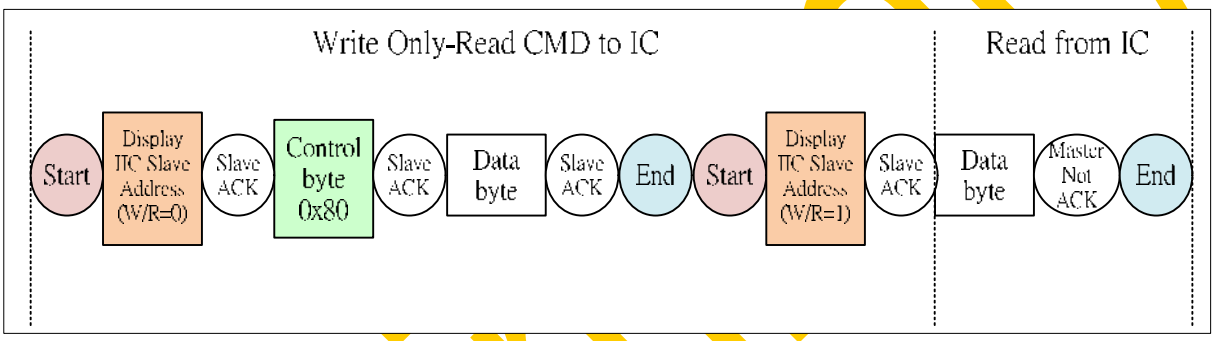


Support read format as below:

1. Read Status



2. Read Only-Read CMD



Note. A0 pin(SA0) pull low, Slave address is 0x78(write) and 0x79(read);
A0 pin(SA0) pull high, Slave address is 0x7A(write) and 0x7B(read).

6.7. Access to Display Data RAM and Internal Registers

This module determines whether the input data is interpreted as data or command. When A0 = “H”, the inputs at D7 - D0 are interpreted as data and be written to display RAM. When A0 = “L”, the inputs at D7 - D0 are interpreted as command, they will be decoded and be written to the corresponding command registers.

6.7.1. Display Data RAM

The Display Data RAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 160 X 160 X 4 bits as shown in Figure 18. For mechanical flexibility, re-mapping on both segment and common outputs can be selected by software.

SEG Scan Direction		A0H (Normal)	SEG0	SEG1	SEG2	SEG3	---	SEG 158	SEG 159
COM Scan Direction		A1H (Remap)	SEG159	SEG158	SEG157	SEG156	---	SEG 1	SEG 0
C0H (Normal)	C8H (Reverse)	Column / Row	00H		01H		---	4FH	
COM0	COM159	00H	D0[3:0]	D0[7:4]	D1[3:0]	D1[7:4]	---	D79[3:0]	D79[7:4]
COM1	COM158	01H	D80[3:0]	D80[7:4]	D81[3:0]	D81[7:4]	---	D159[3:0]	D159[7:4]
COM2	COM157	02H	D160[3:0]	D160[7:4]	D161[3:0]	D161[7:4]	---	D239[3:0]	D239[7:4]
COM3	COM156	03H	D240[3:0]	D240[7:4]	D241[3:0]	D241[7:4]	---	D319[3:0]	D319[7:4]
---		---							
COM156	COM3	9CH	D12480[3:0]	D12480[7:4]	D12481[3:0]	D12481[7:4]	---	D12559[3:0]	D12559[7:4]
COM157	COM2	9DH	D12560[3:0]	D12560[7:4]	D12561[3:0]	D12561[7:4]	---	D12639[3:0]	D12639[7:4]
COM158	COM1	9EH	D12640[3:0]	D12640[7:4]	D12641[3:0]	D12641[7:4]	---	D12719[3:0]	D12719[7:4]
COM159	COM0	9FH	D12720[3:0]	D12720[7:4]	D12721[3:0]	D12721[7:4]	---	D12799[3:0]	D12799[7:4]

Figure 18 Horizontal Addressing Mode

Grayscale Display

SEG Scan Direction / COM Scan Direction		A0H (Normal)	SEG0	SEG1	SEG2	SEG3	---	SEG 158	SEG 159
		A1H (Remap)	SEG159	SEG158	SEG157	SEG156	---	SEG 1	SEG 0
C0H (Normal)	C8H (Reverse)	Column / Row	00H		01H		---	4FH	
COM0	COM159	00H	D0[3:0]	D0[7:4]	D1[3:0]	D1[7:4]	---	D79[3:0]	D79[7:4]
COM1	COM158	01H	D80[3:0]	D80[7:4]	D81[3:0]	D81[7:4]	---	D159[3:0]	D159[7:4]
COM2	COM157	02H	D160[3:0]	D160[7:4]	D161[3:0]	D161[7:4]	---	D239[3:0]	D239[7:4]
COM3	COM156	03H	D240[3:0]	D240[7:4]	D241[3:0]	D241[7:4]	---	D319[3:0]	D319[7:4]
---		---	----------						
COM156	COM3	9CH	D12480[3:0]	D12480[7:4]	D12481[3:0]	D12481[7:4]	---	D12559[3:0]	D12559[7:4]
COM157	COM2	9DH	D12560[3:0]	D12560[7:4]	D12561[3:0]	D12561[7:4]	---	D12639[3:0]	D12639[7:4]
COM158	COM1	9EH	D12640[3:0]	D12640[7:4]	D12641[3:0]	D12641[7:4]	---	D12719[3:0]	D12719[7:4]
COM159	COM0	9FH	D12720[3:0]	D12720[7:4]	D12721[3:0]	D12721[7:4]	---	D12799[3:0]	D12799[7:4]

6.7.2. Vertical addressing mode

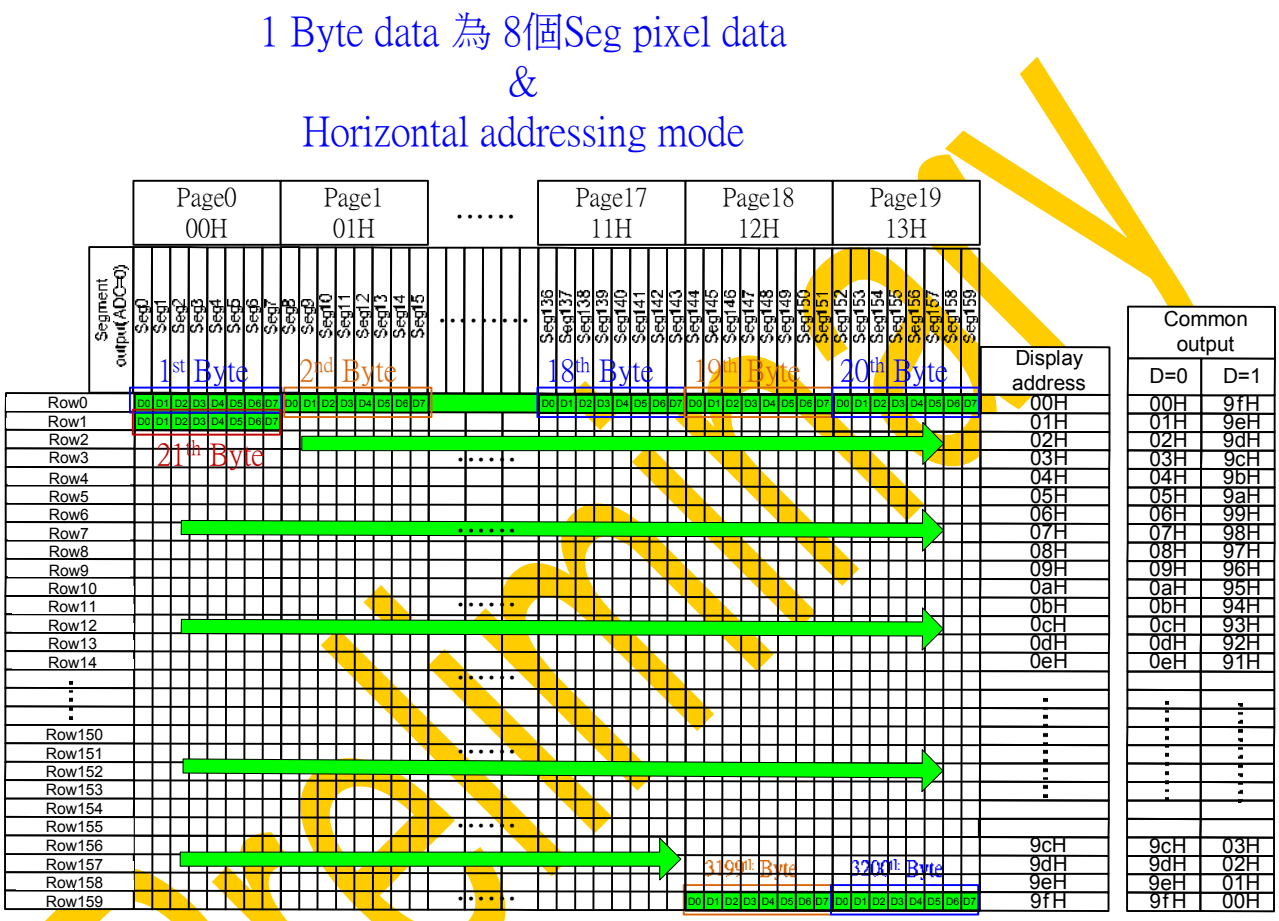
SEG Scan Direction / COM Scan Direction		A0H (Normal)	SEG0	SEG1	SEG2	SEG3	---	SEG 158	SEG 159
		A1H (Remap)	SEG159	SEG158	SEG157	SEG156	---	SEG 1	SEG 0
C0H (Normal)	C8H (Reverse)	Column / Row	00H		01H		---	4FH	
COM0	COM159	00H	D0[3:0]	D0[7:4]	D160[3:0]	D160[7:4]	---	D12640[3:0]	D12640[7:4]
COM1	COM158	01H	D1[3:0]	D1[7:4]	D161[3:0]	D161[7:4]	---	D12641[3:0]	D12641[7:4]
COM2	COM157	02H	D2[3:0]	D2[7:4]	D162[3:0]	D162[7:4]	---	D12642[3:0]	D12642[7:4]
COM3	COM156	03H	D3[3:0]	D3[7:4]	D163[3:0]	D163[7:4]	---	D12643[3:0]	D12643[7:4]
---		---							
COM156	COM3	9CH	D156[3:0]	D156[7:4]	D316[3:0]	D316[7:4]	---	D12796[3:0]	D12796[7:4]
COM157	COM2	9DH	D157[3:0]	D157[7:4]	D317[3:0]	D317[7:4]	---	D12797[3:0]	D12797[7:4]
COM158	COM1	9EH	D158[3:0]	D158[7:4]	D318[3:0]	D318[7:4]	---	D12798[3:0]	D12798[7:4]
COM159	COM0	9FH	D159[3:0]	D159[7:4]	D319[3:0]	D319[7:4]	---	D12799[3:0]	D12799[7:4]

Grayscale Display

SEG Scan Direction / COM Scan Direction		A0H (Normal)	SEG0	SEG1	SEG2	SEG3	---	SEG 158	SEG 159
		A1H (Remap)	SEG159	SEG158	SEG157	SEG156	---	SEG 1	SEG 0
C0H (Normal)	C8H (Reverse)	Column / Row	00H		01H		---	4FH	
COM0	COM159	00H	D0[3:0]	D0[7:4]	D160[3:0]	D160[7:4]	---	D12640[3:0]	D12640[7:4]
COM1	COM158	01H	D1[3:0]	D1[7:4]	D161[3:0]	D161[7:4]	---	D12641[3:0]	D12641[7:4]
COM2	COM157	02H	D2[3:0]	D2[7:4]	D162[3:0]	D162[7:4]	---	D12642[3:0]	D12642[7:4]
COM3	COM156	03H	D3[3:0]	D3[7:4]	D163[3:0]	D163[7:4]	---	D12643[3:0]	D12643[7:4]
---		---	----------						
COM156	COM3	9CH	D156[3:0]	D156[7:4]	D316[3:0]	D316[7:4]	---	D12796[3:0]	D12796[7:4]
COM157	COM2	9DH	D157[3:0]	D157[7:4]	D317[3:0]	D317[7:4]	---	D12797[3:0]	D12797[7:4]
COM158	COM1	9EH	D158[3:0]	D158[7:4]	D318[3:0]	D318[7:4]	---	D12798[3:0]	D12798[7:4]
COM159	COM0	9FH	D159[3:0]	D159[7:4]	D319[3:0]	D319[7:4]	---	D12799[3:0]	D12799[7:4]

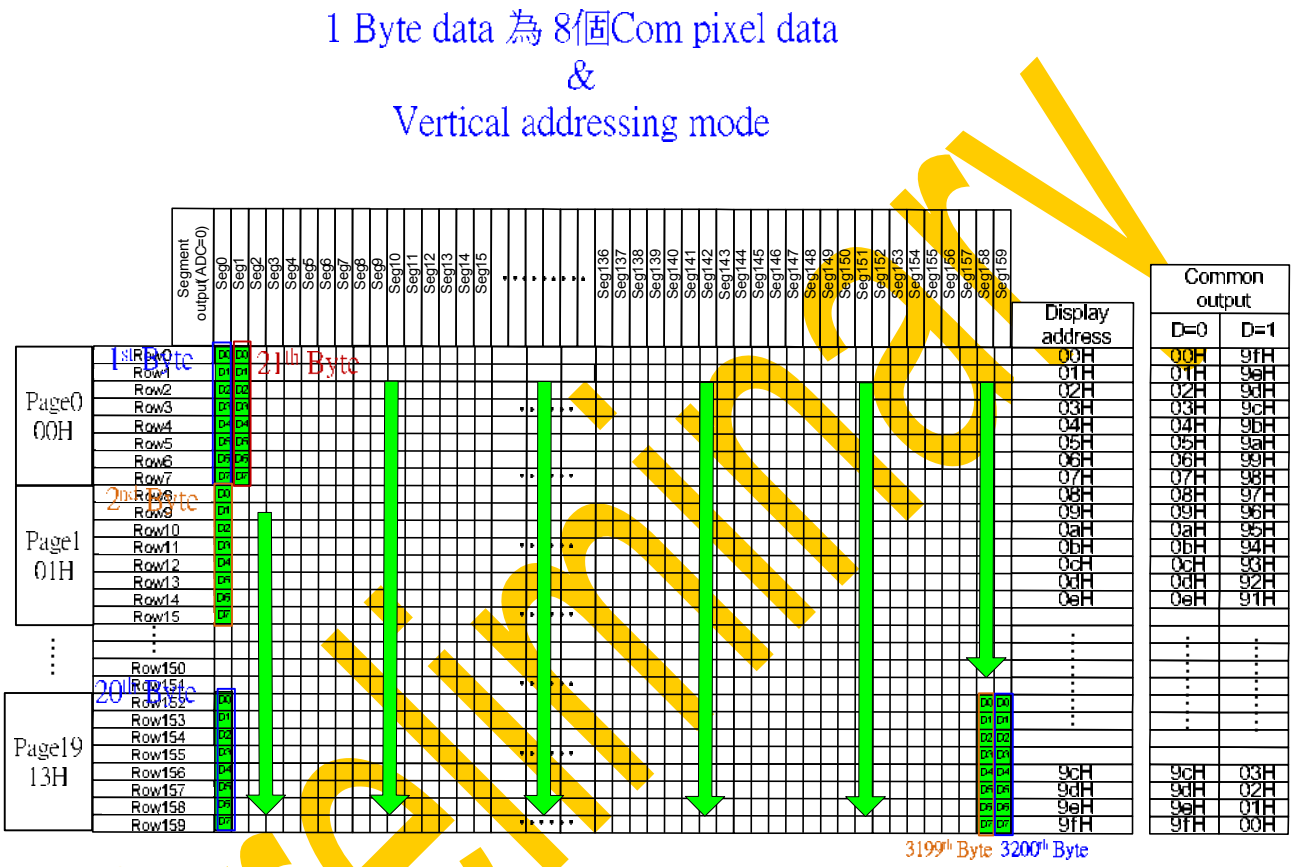
6.7.3. 1 bit Mode Mono Display (1 Byte data composed of 8 Seg pixel data, Horizontal addressing mode)

Register setting : ACh= 0x01, 20h= 0x00
(21H column address setting between 0x00 ~ 0x27; 22H row address setting between 0x00 ~ 0x4F;
21H Column end – Column start +1 must be even value)



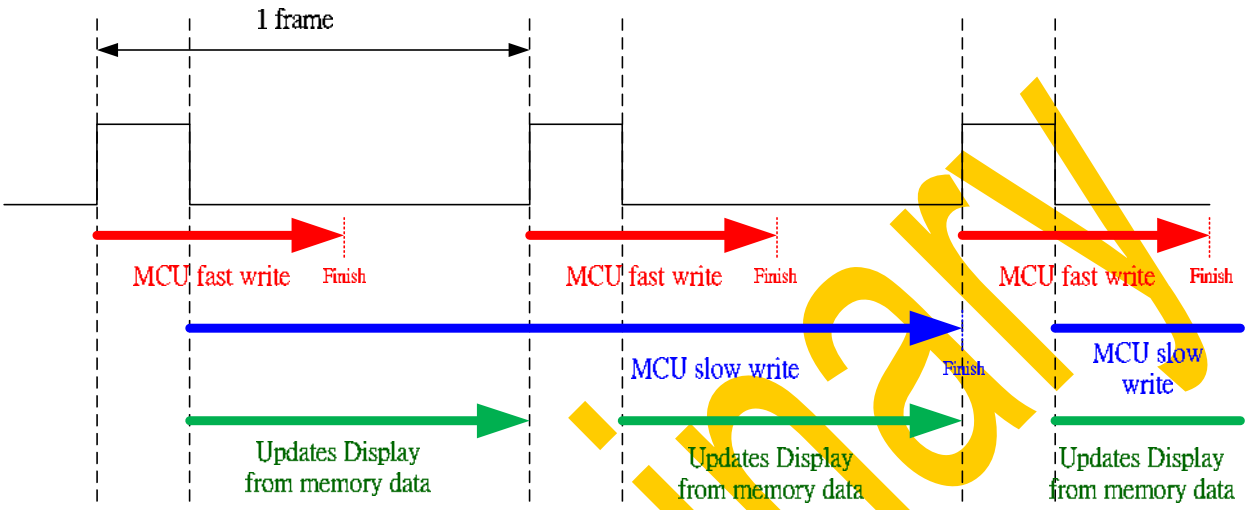
6.7.4. 1 bit Mode Mono Display (1 Byte data composed of 8 Com pixel data, Vertical addressing mode)

Register setting : ACh= 0x03, 20h= 0x00
(21H column address setting between 0x00 ~ 0x27; 22H row address setting between 0x00 ~ 0x4F;
21H Column end – Column start +1 must be even value)



6.8. FRM Synchronization

FRM synchronization signal can be used to prevent tearing effect.



MCU fast write : MCU should start to write new frame of ram data just after rising edge of FRM pulse and should be finished well before the rising edge of the next FRM pulse

MCU slow write : MCU should start to write new frame of ram data just after the falling edge of the 1st FRM pulse and must be finished well before the rising edge of the 3rd FRM pulse

6.9. The Oscillator Circuit

This is a RC type oscillator (Figure 20) that produces the display clock. The oscillator circuit is only enabled when CLS = “H”. When CLS = “L”, the oscillation is off and the display clock comes from the CL pad.

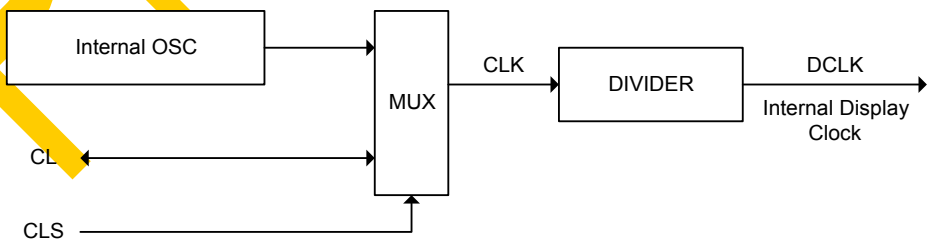


Figure 19

6.10. Current Control and Voltage Control

VPP is from external power supplies. I_{REF} is a reference current source for segment current drivers, it can change the brightness of the screen and the value depends on the resistance of R I_{REF} and VPP.

When VPP=15V, contrast = 0xff, the value of resistor R I_{REF} can be found as Table 9:

Table 9

R I_{REF}	I_{SEG}(uA)
1.3M	300
910K	400
750K	500
560K	600

6.11. Common Drivers/Segment Drivers

Segment drivers deliver 160 current sources to drive OLED panel. The driving current can be adjusted up to 600μA with 256 steps. Common drivers generate voltage scanning pulses.

6.12. 16 Grayscale

The gray scale effect is generated by controlling the pulse width (PW) of current drive phase. The Gray Scale Table stores the corresponding gray scale setting of the 16 gray scale levels (GS0~GS15) through the software commands B8h and BAh.
As shown in Table10, RAM data has 4 bits, represent the 16 gray scale levels from GS0 to GS15.

Note: GS0 cannot be adjusted.

Table 10

RAM Data(4 bits)	Gamma Setting (Command B8h)	Default Gamma Setting for PWM-driving (Command BAh)
0000	GS0	GP0
0001	GS1	GP1
0010	GS2	GP2
…	…	…
1110	GS14	GP14
1111	GS15	GP15

6.13. Reset Circuit

When power is turned on or the RESB input falls to “L”, these reenter their default state.

The default settings are shown below:

1. Display is OFF. Common and segment are in high impedance state.
2. 160 X 160 Display mode.
3. Normal segment and display data mapping (SEG0 is mapped to the top line of the display).
4. Shift register data clear in serial interface.
5. Column address counter is set at 0.
6. Contrast control register is set at 80H.
7. Normal common scan direction

7. Commands

The CH1120 uses a combination of A0, $\overline{RD}$ (E) and $\overline{WR}$ (R / $\overline{W}$) signals to identify data bus signals. As the chip analyzes and executes each command using internal timing clock only regardless of external clock, its processing speed is very high and its busy check is usually not required. The 8080 series microprocessor interface enters a read status when a low pulse is input to the $\overline{RD}$ pad and a write status when a low pulse is input to the $\overline{WR}$ pad. The 6800 series microprocessor interface enters a read status when a high pulse is input to the R / $\overline{W}$ pad and a write status when a low pulse is input to this pad. When a high pulse is input to the E pad, the command is activated. (For timing, see AC Characteristics.). Accordingly, in the command explanation and command table, $\overline{RD}$ (E) becomes 1(HIGH) when the 6800 series microprocessor interface reads status of display data. This is an only different point from the 8080 series microprocessor interface.

Taking the 8080 series, microprocessor interface as an example command will explain below. When the serial interface is selected, the input data is starting from D7 in sequence.

7.1. Command Set

7.1.1. Set Lower Column Start Address: (00H - 0FH)

7.1.2. Set Higher Column Start Address: (10H - 14H)

Specify column address of display RAM. Divide the column address into 4 higher bits and 4 lower bits. Set each of them into successions. When the microprocessor repeats to access to the display RAM, the column address counter is incremented during each access until address 4FH is accessed (In horizontal addressing mode). Whenever the column address pointer finishes accessing the end column address, it is reset back to start column address and the row address is incremented to the next row.

	A0	$\overline{RD}$ (E)	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
Column Start High bits	0	1	0	0	0	0	1	0	A6	A5	A4
Column Start Low bits	0	1	0	0	0	0	0	A3	A2	A1	A0

A6	A5	A4	A3	A2	A1	A0	Display address
0	0	0	0	0	0	0	0 (Column Start default)
0	0	0	0	0	0	1	1
			:				:
1	0	0	1	1	1	0	4EH
1	0	0	1	1	1	1	4FH

Note: Don't use any commands not mentioned above.

This command cannot be used if user has written the CMD 21H for column start and end address.

7.1.3. Set Row Start Address of Display RAM: (B0H) (Double Bytes Command)

Specify Row address to load display RAM data to Row address register. Any RAM data bit can be accessed when its row address and column address are specified. The display remains unchanged even when the Row address is changed.

■ Row address Mode Setting: (B0H)

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R/$\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	1	0	0	0	0

■ Row address setting:

	A0	$\overline{RD}$ (E)	$\overline{WR}$ (R/$\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
Row Start	0	1	0	A7	A6	A5	A4	A3	A2	A1	A0

A7	A6	A5	A4	A3	A2	A1	A0	Row address
0	0	0	0	0	0	0	0	0 (Row Start default)
0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	1	0	2
0	0	0	0	0	0	1	1	3
	…	…	…	…	…	…	…	…
1	0	0	1	1	1	0	1	9DH
1	0	0	1	1	1	1	0	9EH
1	0	0	1	1	1	1	1	9FH

Note: Don't use any commands not mentioned above.

This command cannot be used if user has written the CMD 22H for column start and end address.

7.1.4. Set Column Start and End Address : (21H)

This triple byte command specifies column start address and end address of the display data RAM. This command also sets the column address pointer to column start address. This pointer is used to define the current read/write column address in graphic display data RAM. In horizontal addressing mode, after finishing read/write one column data, it is incremented automatically to the next column address. Whenever the column address pointer finishes accessing the end column address, it is reset back to start column address and the row address is incremented to the next row.

	A0	$\overline{RD}$ (E)	$\overline{WR}$ (R/$\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
	0	1	0	0	0	1	0	0	0	0	1
Column Start	0	1	0	*	A6	A5	A4	A3	A2	A1	A0
Column End	0	1	0	*	B6	B5	B4	B3	B2	B1	B0

A6	A5	A4	A3	A2	A1	A0	Display address
0	0	0	0	0	0	0	0 (Column Start default)
0	0	0	0	0	0	1	1
			:				:
1	0	0	1	1	1	0	4EH
1	0	0	1	1	1	1	4FH

B6	B5	B4	B3	B2	B1	B0	Display address
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
			:				:
1	0	0	1	1	1	0	4EH
1	0	0	1	1	1	1	4FH (Column End default)

7.1.5. Set Row Start and End Address: (22H)

This triple byte command specifies row start address and end address of the display data RAM. This command also sets the row address pointer to row start address. This pointer is used to define the current read/write row address in graphic display data RAM. In vertical addressing mode, after finishing read/write one row data, it is incremented automatically to the next row address. Whenever the row address pointer finishes accessing the end row address, it is reset back to start row address and the column address is incremented to the next column.

	A0	$\overline{RD}$ (E)	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
	0	1	0	0	0	1	0	0	0	1	0
Row Start	0	1	0	A7	A6	A5	A4	A3	A2	A1	A0
Row End	0	1	0	B7	B6	B5	B4	B3	B2	B1	B0

A7	A6	A5	A4	A3	A2	A1	A0	Display address
0	0	0	0	0	0	0	0	0 (Row Start default)
0	0	0	0	0	0	0	1	1
				:				:
1	0	0	1	1	1	1	0	9EH
1	0	0	1	1	1	1	1	9FH

B7	B6	B5	B4	B3	B2	B1	B0	Display address
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
				:				:
1	0	0	1	1	1	1	0	9EH
1	0	0	1	1	1	1	1	9FH (Row End default)

		SEG0	SEG1	SEG2	SEG3	---	SEG156	SEG157	SEG158	SEG159
	Address	00H		01H		---	4FH		4FH	
COM0	00H									
COM1	01H									
COM2	02H									
COM3	03H									
---	---									
COM156	9CH									
COM157	9DH									
COM158	9EH									
COM159	9FH									

Figure 14 Column and Row Address Pointer Movement

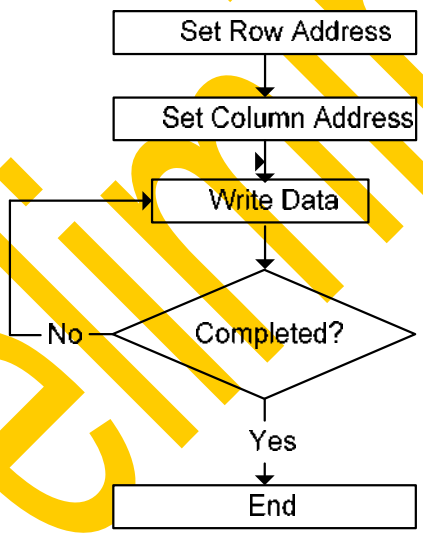


Figure 14 Write Ram flow

Once writing CMD column start address and row start address for writing data to ram or reading data from ram, the position of ram for writing or reading should be pointed to the row & column start address setting. In horizontal addressing mode, after writing data to ram or reading data from ram, the column address will increase one automatically. When the column address reaches the column end address, it will be return to column start address and the row address will increase one. In vertical addressing mode, after writing data to ram or reading data from ram, the row address will increase one automatically. When the row address reaches the row end address, it will be return to row start address and the column address will increase one.

7.1.6. Set Memory addressing mode (20H)

There are two different memory addressing modes in CH1120: row addressing mode and vertical addressing mode. This command sets the way of memory addressing into one of the above two modes, “COL” means column.

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R/$\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	0	0	0	0	0
0	1	0	*	*	*	*	*	*	*	D

■ Horizontal addressing mode (D=0) (default)

In Horizontal addressing mode, after the display RAM is read/ written, the column address is increased automatically by 1. If the column address reaches column end address, the column address is reset to column start address and row address is increased automatically by 1. When the Segment is remapped, the direction of both page and byte are reversed. The sequence of movement of the row and column address for row addressing mode is shown in figure 13-1.

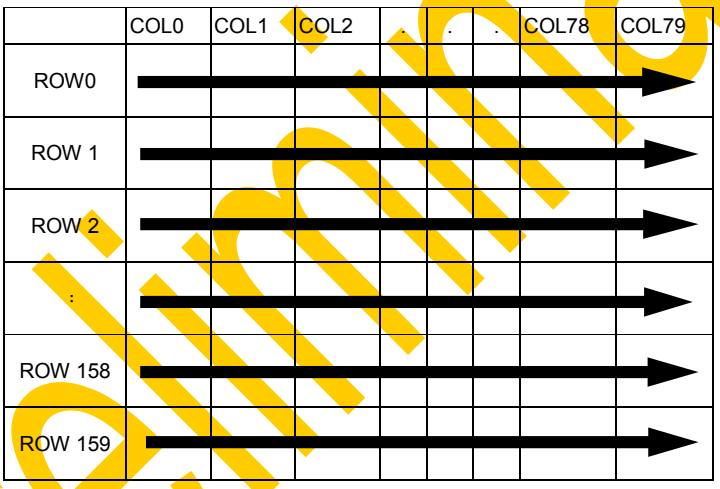


Figure13-1(a)

	Column	SEG0	SEG1	SEG2	SEG3	---	SEG158	SEG159
Row	Address	00H		01H		---	4FH	
COM0	00H	D0[3:0]	D0[7:4]	D1[3:0]	D1[7:4]	---	D79[3:0]	D79[7:4]
COM1	01H	D80[3:0]	D80[7:4]	D81[3:0]	D81[7:4]	---	D159[3:0]	D159[7:4]
COM2	02H	D160[3:0]	D160[7:4]	D161[3:0]	D161[7:4]	---	D239[3:0]	D239[7:4]
COM3	03H	D240[3:0]	D240[7:4]	D241[3:0]	D241[7:4]	---	D319[3:0]	D319[7:4]
---	---							
COM156	9CH	D12480[3:0]	D12480[7:4]	D12481[3:0]	D12481[7:4]	---	D12559[3:0]	D12559[7:4]
COM157	9DH	D12560[3:0]	D12560[7:4]	D12561[3:0]	D12561[7:4]	---	D12639[3:0]	D12639[7:4]
COM158	9EH	D12640[3:0]	D12640[7:4]	D12641[3:0]	D12641[7:4]	---	D12719[3:0]	D12719[7:4]
COM159	9FH	D12720[3:0]	D12720[7:4]	D12721[3:0]	D12721[7:4]	---	D12799[3:0]	D12799[7:4]

Figure13-1(b)
Figure13-1 Horizontal addressing mode (Seg-remap=0)

■ Vertical addressing mode: (D=1)

In vertical addressing mode, after the display RAM is read/ written, the row address is increased automatically by 1. If the row address reaches the row end address, the row address is reset to row start address and column address is increased automatically by 1. When the Segment is remapped, the direction of both page and byte are reversed. The sequence of movement of the page and column address for vertical addressing mode is shown in Figure 13-3.

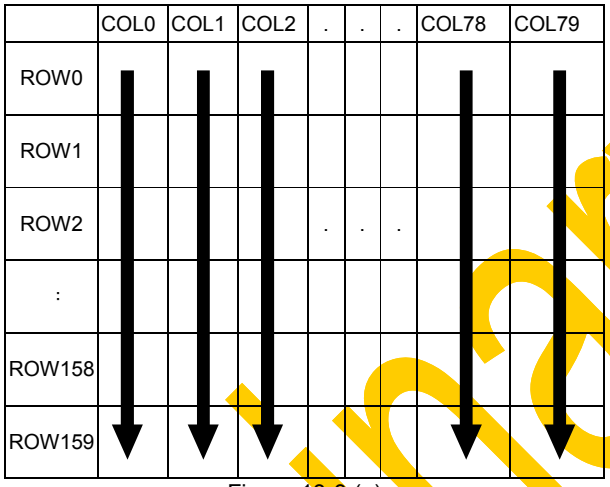


Figure 13-3 (a)

	Column	SEG0	SEG1	SEG2	SEG3	---	SEG158	SEG159
Row	Address	00H		01H		---	4FH	
COM0	00H	D0[3:0]	D0[7:4]	D160[3:0]	D160[7:4]	---	D12640[3:0]	D12640[7:4]
COM1	01H	D1[3:0]	D1[7:4]	D161[3:0]	D161[7:4]	---	D12641[3:0]	D12641[7:4]
COM2	02H	D2[3:0]	D2[7:4]	D162[3:0]	D162[7:4]	---	D12642[3:0]	D12642[7:4]
COM3	03H	D3[3:0]	D3[7:4]	D163[3:0]	D163[7:4]	---	D12643[3:0]	D12643[7:4]
---	---							
COM156	9CH	D156[3:0]	D156[7:4]	D316[3:0]	D316[7:4]	---	D12796[3:0]	D12796[7:4]
COM157	9DH	D157[3:0]	D157[7:4]	D317[3:0]	D317[7:4]	---	D12797[3:0]	D12797[7:4]
COM158	9EH	D158[3:0]	D158[7:4]	D318[3:0]	D318[7:4]	---	D12798[3:0]	D12798[7:4]
COM159	9FH	D159[3:0]	D159[7:4]	D319[3:0]	D319[7:4]	---	D12799[3:0]	D12799[7:4]

Figure13-3 (b)

Figure 13-3 Vertical addressing mode (Seg remap=0)

7.1.7. Set Breathing Display Effect (23H): (Double Bytes Command)

This command set Breathing Display Effect ON/OFF and Time Interval.

- Breathing Display Effect Set: (23H)

A0	$\frac{E}{RD}$	$\frac{R/W}{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	0	0	0	1	1
0	1	0	ON/ OFF	*	*	A4	A3	A2	A1	A0
0	1	0	0	C2	C1	C0	0	B2	B1	B0

- ON/OFF set:

When ON/OFF ="L", Breathing Display Effect OFF. (Default)

When ON/OFF ="H", Breathing Display Effect ON.

- Breathing Display Effect Maximum Brightness Adjust Set: (A4 – A3)

A_4	A_3	Maximum Brightness (Contrast+1)
0	0	256(Default)
0	1	128
1	0	64
1	1	32

- Breathing Display Effect Time Interval Set: (A2 – A0)

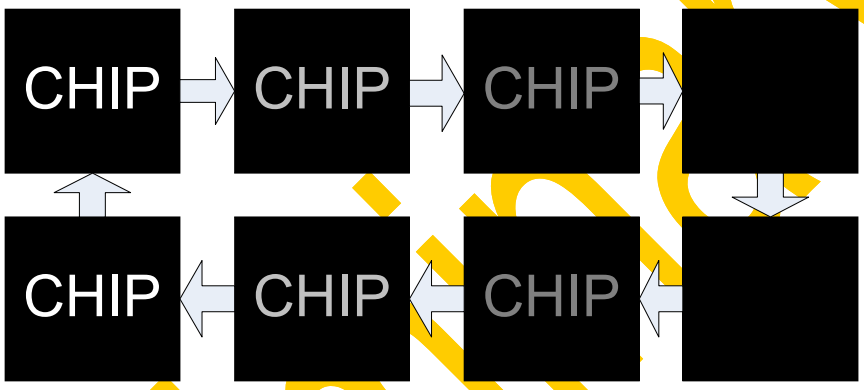
A_2	A_1	A_0	Time Interval step
0	0	0	1 Frames
0	0	1	2 Frames(Default)
0	1	0	3 Frames
:	:	:	:
1	1	0	7 Frames
1	1	1	8 Frames

- Breathing Display t Dark Time Interval Set: (B2 – B0)

B_2	B_1	B_0	Time Interval step
0	0	0	+0 Frame
0	0	1	+25 Frames (Default)
0	1	0	+50 Frames
0	1	1	+100 Frames
1	0	0	+150 Frames
1	0	1	+200 Frames
1	1	0	+250 Frames
1	1	1	+300 Frames

■ Breathing Display Effect Brightest Time Interval Set: (C2 – C0)

C_2	C_1	C_0	Time Interval step
0	0	0	+0Frame (Default)
0	0	1	+25 Frames
0	1	0	+50 Frames
0	1	1	+100 Frames
1	0	0	+150 Frames
1	0	1	+200 Frames
1	1	0	+250 Frames
1	1	1	+300 Frames



7.1.8. Set Horizontal Scroll & Vertical Scroll (24H-27H): (Six Bytes Command)

This command consists of 6 consecutive bytes to set up the horizontal scroll and the vertical scroll parameters. It determined the scrolling start column, end column, start row, end row and time interval.

Before issuing this command, the horizontal scroll must be deactivated (2EH). Otherwise, ram content may be corrupted.

■ Horizontal Scroll & Vertical Scroll Setup Mode Set: (24H-27H)

A0	$\frac{E}{RD}$	$\frac{R/W}{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	0	0	1	D1	D0
0	1	0	A7	A6	A5	A4	A3	A2	A1	A0
0	1	0	B7	B6	B5	B4	B3	B2	B1	B0
0	1	0	C7	C6	C5	C4	C3	C2	C1	C0
0	1	0	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	*	*	*	*	*	E2	E1	E0

D1	D0	Scroll Direction Set
0	0	Scroll Down
0	1	Scroll Up
1	0	Scroll Right(default)
1	1	Scroll Left

■ Start Column Position Set: (A7 – A0)

A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Start Column Position
0	1	0	0	0	0	0	0	0	0	0	0(default)
0	1	0	0	0	0	0	0	0	0	1	1
0	1	0					:				:
0	1	0	1	0	0	1	1	1	1	0	158
0	1	0	1	0	0	1	1	1	1	1	159

■ End Column Position Set: (B7 – B0)

A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	End Column Position
0	1	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	1	1
0	1	0					:				:
0	1	0	1	0	0	1	1	1	1	0	158
0	1	0	1	0	0	1	1	1	1	1	159(default)

■ Start Row Position Set: (C7 – C0)

A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Start Row Position
0	1	0	0	0	0	0	0	0	0	0	0(default)
0	1	0	0	0	0	0	0	0	0	1	1
0	1	0					:				:
0	1	0	1	0	0	1	1	1	1	0	158
0	1	0	1	0	0	1	1	1	1	1	159

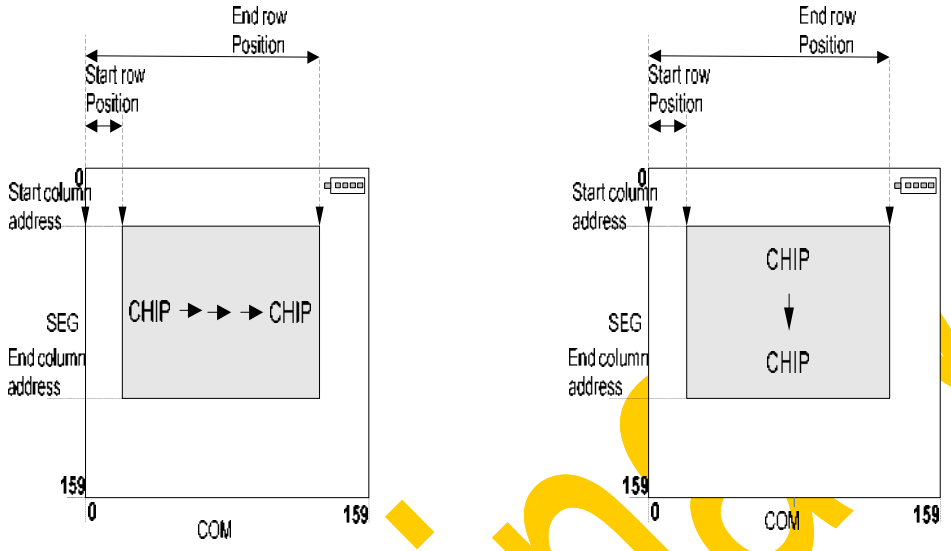
■ End Row Position Set: (D7 – D0)

A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	End Row Position
0	1	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	1	1
0	1	0					:				:
0	1	0	1	0	0	1	1	1	1	0	158
0	1	0	1	0	0	1	1	1	1	1	159 (default)

■ Time Interval Set: (E2 – E0)

A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Time Interval
0	1	0	*	*	*	*	*	0	0	0	6 frames(default)
0	1	0	*	*	*	*	*	0	0	1	32 frames
0	1	0	*	*	*	*	*	0	1	0	64 frames
0	1	0	*	*	*	*	*	0	1	1	128 frames
0	1	0	*	*	*	*	*	1	0	0	3 frames
0	1	0	*	*	*	*	*	1	0	1	4 frames
0	1	0	*	*	*	*	*	1	1	0	5 frames
0	1	0	*	*	*	*	*	1	1	1	2 frames

Note: "*" stands for "Don't care".



Note. Scrolling direction is base on display scrolling.

7.1.9. Set Scroll Mode: (28H–2BH)

Control continuous or single screen scroll.

A0	$\overline{E}$ / $\overline{RD}$	R / $\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	0	1	0	D1	D0

When D0=”L”, Continuous horizontal/vertical scroll. (Default)

When D0=”H”, Single Screen scroll.

When D1=”L”, Disable write 1 Column/Row ram data for scrolling mode. (Default)

When D1=”H”, Enable write 1 Column/Row ram data for scrolling mode.

D1	D0	Scroll mode
0	0	Continuous horizontal/vertical scroll(default)
0	1	Single Screen scroll
1	0	-
1	1	1 Column/Row scroll mode

Note. 1 Column/Row scroll mode function does not support in 1-bit mono mode.

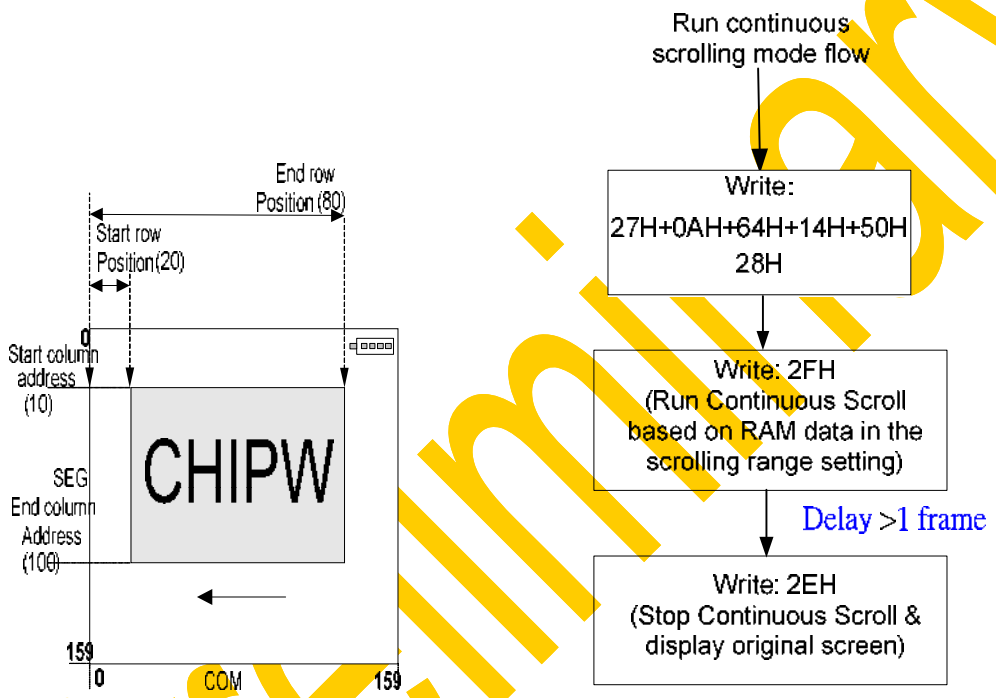
7.1.10. Set 1 Column/Row scroll mode display scroll : (EBH)

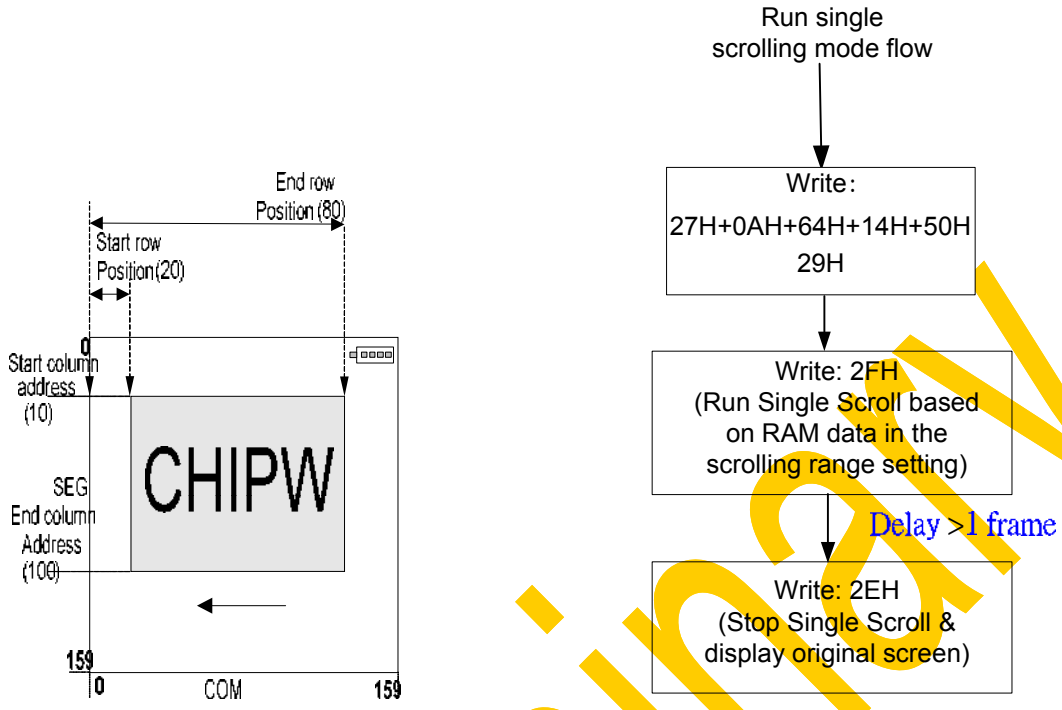
This command is to scroll display in 1 column/row scroll mode.

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	0	1	1
0	1	0	*	*	*	*	*	*	*	D

D=1 , scroll 1 column/row.

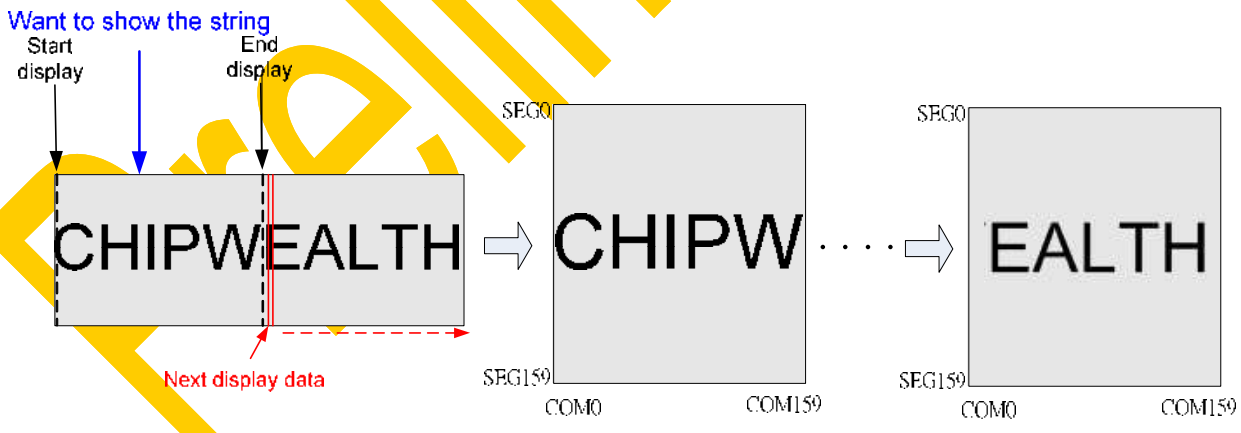
■ Continuous scroll & Single scroll flow





Note: The panel will normally display RAM data after the single screen scroll is over.
The 2EH and 2FH Command must be written for the next single screen scroll.

■ 1 Column/Row scroll flow



Scroll left display example

160x160	Step	24H - Down
1st Scroll	1	24H - 00, 9F, 00, 9F, 00
	2	2BH
	3	2FH
	4	delay >1 frame
	5	20H - 01
	6	21H - 4F, 4F
	7	Write 1x160 Byte
	8	delay >2 frame
	9	EBH - 01
	10	delay >2 frame
	11	EBH - 01
	12	delay >2 frame
2nd Scroll	1	21H - 4E, 4E
	2	Write 1x160 data
	3	delay >2 frame
	4	EBH - 01
	5	delay >2 frame
	6	EBH - 01
	7	delay >2 frame
:		
:		
80th Scroll	1	21H - 00, 00
	2	Write 1x160Byte
	3	delay >2 frame
	4	EBH - 01
	5	delay >2 frame
	6	EBH - 01
	7	delay >2 frame

160x160	Step	25H - Up
1st Scroll	1	25H - 00, 9F, 00, 9F, 00
	2	2BH
	3	2FH
	4	delay >1 frame
	5	20H - 01
	6	21H - 00, 00
	7	Write 1x160 Byte
	8	delay >2 frame
	9	EBH - 01
	10	delay >2 frame
	11	EBH - 01
	12	delay >2 frame
2nd Scroll	1	21H - 01, 01
	2	Write 1x160 Byte
	3	delay >2 frame
	4	EBH - 01
	5	delay >2 frame
	6	EBH - 01
	7	delay >2 frame
:		
:		
80th Scroll	1	21H - 4F, 4F
	2	Write 1x160 Byte
	3	delay >2 frame
	4	EBH - 01
	5	delay >2 frame
	6	EBH - 01
	7	delay >2 frame

160x160	Step	26H - Right
1st Scroll	1	26H - 00, 9F, 00, 9F, 00
	2	2BH
	3	2FH
	4	delay >1 frame
	5	22H - 9F, 9F
	6	Write 160x1 Byte
	7	delay >2 frame
	8	EBH - 01
	9	delay >2 frame
2nd Scroll	1	22H - 9E, 9E
	2	Write 160x1 Byte
	3	delay >2 frame
	4	EBH - 01
	5	delay >2 frame
:		:
160th Scroll	1	22H - 00, 00
	2	Write 160x1 Byte
	3	delay >2 frame
	4	EBH - 01
	5	delay >2 frame

160x160	Step	27H - Left
1st Scroll	1	27H - 00, 9F, 00, 9F, 00
	2	2BH
	3	2FH
	4	delay >1 frame
	5	22H - 00, 00
	6	Write 160x1 Byte
	7	delay >2 frame
	8	EBH - 01
	9	delay >2 frame
2nd Scroll	1	22H - 01, 01
	2	Write 160x1 Byte
	3	delay >2 frame
	4	EBH - 01
	5	delay >2 frame
:		:
160th Scroll	1	22H - 9F, 9F
	2	Write 160x1 Byte
	3	delay >2 frame
	4	EBH - 01
	5	delay >2 frame

7.1.11. Set Deactivate /Activate Scroll: (2EH - 2FH)

Stop or start motion of horizontal/vertical scrolling. This command should only be issued after horizontal/vertical scroll setup parameters (24H/25H/26H/27H/28H/29H/2BH) are defined. The delay time >1 frame between 2EH and 2FH is necessary.

A0	E / $\overline{RD}$	R/W / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	0	1	1	1	D

When D="L", Stop motion of horizontal scroll. (default)

When D="H", Start motion of horizontal scroll.

Valid command sequence 1: 2Eh, delay>1 frame, 24h, XXh, XXh, XXh, XXh, XXh, 28h or 29h or 2Bh, 2Fh, delay > 1 frame, 2Eh.

Valid command sequence 2: 2Eh, delay>1 frame, 25h, XXh, XXh, XXh, XXh, XXh, 28h or 29h or 2Bh, 2Fh, delay > 1 frame, 2Eh.

Valid command sequence 3: 2Eh, delay>1 frame, 26h, XXh, XXh, XXh, XXh, XXh, 28h or 29h or 2Bh, 2Fh, delay > 1 frame, 2Eh.

Valid command sequence 4: 2Eh, delay>1 frame, 27h, XXh, XXh, XXh, XXh, XXh, 28h or 29h or 2Bh, 2Fh, delay > 1 frame, 2Eh.

Note: The following actions are prohibited after the horizontal scroll is activated

- Changing additional horizontal scroll setup parameters.
- Changing horizontal scroll setup parameters.
- Changing continuous or single screen scroll setup parameters.

After the deactivating horizontal scroll issued, the display of screen is reset to original status.

7.1.12. Set Partial Display Mode: (2CH-2DH) (Five Bytes Command)

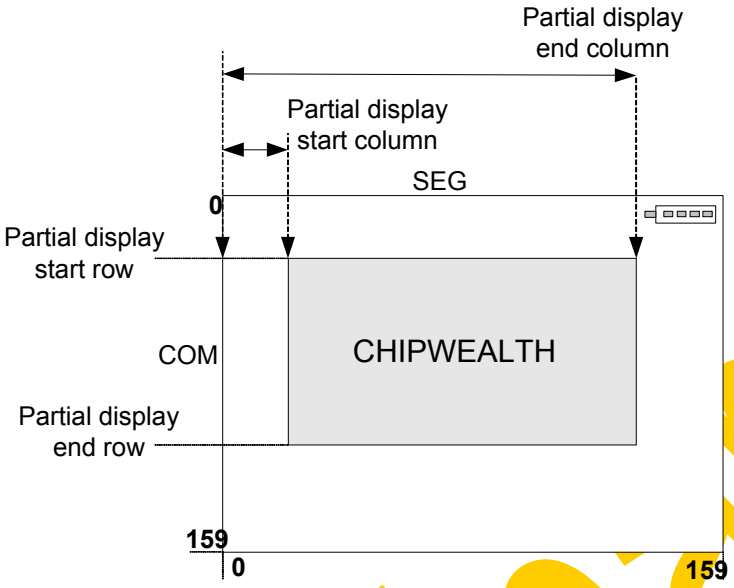
This command consists of 6 consecutive bytes to set up the display area in column start/end address and row start/end address. When D0=1(CMD 2DH), the partial display mode is enable. When partial display mode is enable, display start line (A2h) must be default value.

- Partial Display Mode Set: (2CH – 2DH)

	A0	E / $\overline{RD}$	R/W / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
	0	1	0	0	0	1	0	1	1	0	D0
Column Start	0	1	0	A7	A6	A5	A4	A3	A2	A1	A0
Column End	0	1	0	B7	B6	B5	B4	B3	B2	B1	B0
Row Start	0	1	0	C7	C6	C5	C4	C3	C2	C1	C0
Row End	0	1	0	D7	D6	D5	D4	D3	D2	D1	D0

When D0="L", Partial display mode off. (default)

When D0="H", Partial display mode on.



7.1.13. Set Contrast Control Register: (81H) (Double Bytes Command)

This command is to set contrast setting of the display. The chip has 256 contrast steps from 00 to FF. The segment output current increases as the contrast step value increases. Segment output current setting: ISEG = α/256 X IREF X scale factor

Where: α is contrast step; IREF is reference current equals 18.75μA; Scale factor = 32

■ The Contrast Control Mode Set: (81H)

When this command is input, the contrast data register set command becomes enabled. Once the contrast control mode has been set, no other command except for the contrast data register command can be used. Once the contrast data set command has been used to set data into the register, then the contrast control mode is released.

A0	E / $\overline{RD}$	R / $\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	0	0	0	0	1
0	1	0	A7	A6	A5	A4	A3	A2	A1	A0

■ Contrast Data Register Set: (00H - FFH)

By using this command to set eight bits of data to the contrast data register; the OLED segment output assumes one of the 256 current levels. When this command is input, the contrast control mode is released after the contrast data register has been set.

A0	E / $\overline{RD}$	R / $\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	I_{SEG}
0	1	0	0	0	0	0	0	0	0	0	Small
0	1	0	0	0	0	0	0	0	0	1	
0	1	0	0	0	0	0	0	0	1	0	
0	1	0					:				:
0	1	0	1	0	0	0	0	0	0	0	DEFAULT
0	1	0					:				:
0	1	0	1	1	1	1	1	1	1	0	

0	1	0	1	1	1	1	1	1	1	1	Large

When the contrast control function is not used, set the D7 - D0 to 1000,0000.

7.1.14. Set Display Start Line: (A2H) (Double Bytes Command)

Specifies line address determine the initial display line or COM0. The RAM display data becomes the top line of OLED screen. It is followed by the higher number of lines in ascending order, corresponding to the duty cycle. When this command changes the line address, the smooth scrolling or page change takes place.

- The Display Start line Mode Set: (A2H)

A0	$\frac{E}{RD}$	$\frac{R/W}{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	1	0	0	0	0	0	0

- The Display Start line Register Set: (00H –9FH)

A0	$\frac{E}{RD}$	$\frac{R/W}{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	COMx
0	1	0	0	0	0	0	0	0	0	0	0(default)
0	1	0	0	0	0	0	0	0	0	1	1
0	1	0	0	0	0	0	0	0	1	0	2
0	1	0	:								:
0	1	0	1	0	0	0	0	0	0	0	128
0	1	0	:								:
0	1	0	1	0	0	1	1	1	1	0	158
0	1	0	1	0	0	1	1	1	1	1	159

COM pin	Multiplex ratio (A8) = 9Fh		Multiplex ratio (A8) = 7Fh	
	Display start line(A2H) =00h	Display start line(A2H) =0Ah	Display start line(A2H) =00h	Display start line(A2H) =0Ah
COM0	Row 0	Row 10	Row 0	Row 10
COM1	Row 1	Row 11	Row 1	Row 11
COM2	Row 2	Row 12	Row 2	Row 12
COM3	Row 3	Row 13	Row 3	Row 13
:	:	:	:	:
:	:	:	:	:
COM116	Row 116	Row 126	Row 116	Row 126
COM117	Row 117	Row 127	Row 117	Row 127
COM118	Row 118	Row 128	Row 118	Row 128
COM119	Row 119	Row 129	Row 119	Row 129
:	:	:	:	:
COM125	Row 125	Row 135	Row 125	Row 135
COM126	Row 126	Row 136	Row 126	Row 136
COM127	Row 127	Row 137	Row 127	Row 137
COM128	Row 128	Row 138	-	-
COM129	Row 129	Row 139	-	-
COM130	Row 130	Row 140	-	-
:	:	:	:	:
COM146	Row 146	Row 156	-	-
COM147	Row 147	Row 157	-	-
COM148	Row 148	Row 158	-	-
COM149	Row 149	Row 159	-	-
COM150	Row 150	Row 0	-	-
COM151	Row 151	Row 1	-	-
:	:	:	:	:
COM156	Row 156	Row 6	-	-
COM157	Row 157	Row 7	-	-
COM158	Row 158	Row 8	-	-
COM159	Row 159	Row 9	-	-

Display start line COM output (C0H - COM0 to COM [N -1])

COM pin	Multiplex ratio (A8) = 9Fh		Multiplex ratio (A8) = 7Fh	
	Display start line(A2H) =00h	Display start line(A2H) =0Ah	Display start line(A2H) =00h	Display start line(A2H) =0Ah
COM0	Row 159	Row 9	Row 127	Row 137
COM1	Row 158	Row 8	Row 126	Row 136
COM2	Row 157	Row 7	Row 125	Row 135
COM3	Row 156	Row 6	Row 124	Row 134
:	:	:	:	:
COM8	Row 151	Row 1	Row 119	Row 129
COM9	Row 150	Row 0	Row 118	Row 128
COM10	Row 149	Row 159	Row 117	Row 127
COM11	Row 148	Row 158	Row 116	Row 126
:	:	:	:	:
:	:	:	:	:
COM116	Row 43	Row 53	Row 11	Row 21
COM117	Row 42	Row 52	Row 10	Row 20
COM118	Row 41	Row 51	Row 9	Row 19
COM119	Row 40	Row 50	Row 8	Row 18
:	:	:	:	:
COM125	Row 34	Row 44	Row 2	Row 12
COM126	Row 33	Row 43	Row 1	Row 11
COM127	Row 32	Row 42	Row 0	Row 10
COM128	Row 31	Row 41	-	-
COM129	Row 30	Row 40	-	-
COM130	Row 29	Row 39	-	-
:	:	:	:	:
COM146	Row 13	Row 23	-	-
COM147	Row 12	Row 22	-	-
COM148	Row 11	Row 21	-	-
COM149	Row 10	Row 20	-	-
COM150	Row 9	Row 19	-	-
COM151	Row 8	Row 18	-	-
:	:	:	:	:
COM156	Row 3	Row 13	-	-
COM157	Row 2	Row 12	-	-
COM158	Row 1	Row 11	-	-
COM159	Row 0	Row 10	-	-

Display start line COM output (C8H - COM [N -1] to COM0)

7.1.15. Set External or internal I_{REF} : (ADH)

IREF can be controlled by external resister or internal resister.

■ IREF Resister Set: (ADH)

A0	$\frac{E}{RD}$	$\frac{R/W}{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	1	0	1
0	1	0	MS_SEL	CMD_MODE	*	*	iseg_hw_adj_en	D2	D1	D0

When D2 = “L”, External resistor is selected(default).

When D2 = “H”, Internal resistor is selected.

■ Internal Resister Set: (A1 – A0)

D1	D0	I_{SEG}(uA)
0	0	300
0	1	400
1	0	500(default)
1	1	600

When VPP=15V,Contrast=256, RIref & I_{REF} Table(Just for reference):

R I_{REF}	I_{SEG}(uA)
1.3M	300
910K	400
750K	500
560K	600

Note: IREF = (VPP-2V) / RIref

■ Adjust ISEG(Contrast register 81h) individual for Master IC or Slave IC.

When CMD_MODE = “L”, Master IC & Slave IC accept contrast register cmd. (default).

When CMD_MODE = “H”, Select Master IC or Slave IC accept contrast register cmd.

When MS_SEL = “L”, Slave IC selected.

When MS_SEL = “H”, Master IC selected.

MS_SEL	CMD_MODE	Select IC
0	0	Master & Slave (default)
0	1	Slave
1	0	Master & Slave
1	1	Master

■ Adjust ISEG by PAD[7:3]

When iseg_hw_adj_en = “L”, Disable ISEG adjust. (default).

When iseg_hw_adj_en = “H”, Enable ISEG adjust.

To change ISEG is to modify the value of D3-D7 pin.

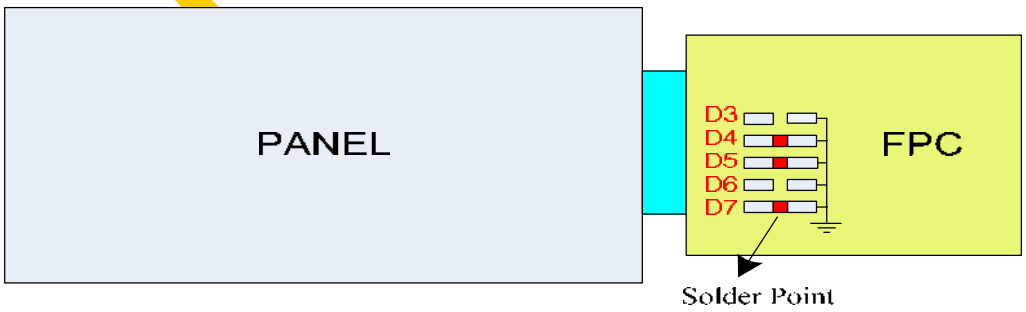
Step number	D7	D6	D5	D4	D3	Contrast code (81H)

Up	0	0	0	0	0	0	Register 81H value
	1	0	0	0	0	1	81H value + 3
	2	0	0	0	1	0	81H value + 6
	3	0	0	0	1	1	81H value + 9
	4	0	0	1	0	0	81H value +12
	5	0	0	1	0	1	81H value +15
	6	0	0	1	1	0	81H value +18
	7	0	0	1	1	1	81H value +21
	8	0	1	0	0	0	81H value +24
	9	0	1	0	0	1	81H value +27
	10	0	1	0	1	0	81H value +30
	11	0	1	0	1	1	81H value +33
	12	0	1	1	0	0	81H value +36
	13	0	1	1	0	1	81H value +39
	14	0	1	1	1	0	81H value +42
	15	0	1	1	1	1	81H value +45
Down	0	1	0	0	0	0	Register 81H value
	1	1	0	0	0	1	81H value - 3
	2	1	0	0	1	0	81H value - 6
	3	1	0	0	1	1	81H value - 9
	4	1	0	1	0	0	81H value - 12
	5	1	0	1	0	1	81H value - 15
	6	1	0	1	1	0	81H value -18
	7	1	0	1	1	1	81H value - 21
	8	1	1	0	0	0	81H value - 24
	9	1	1	0	0	1	81H value - 27
	10	1	1	0	1	0	81H value - 30
	11	1	1	0	1	1	81H value - 33
	12	1	1	1	0	0	81H value - 36
	13	1	1	1	0	1	81H value - 39
	14	1	1	1	1	0	81H value - 42
	15	1	1	1	1	1	81H value - 45

Note1: When 8080/6800 interface is used, ISEG adjust is disabled.

Note2: When ISEG adjust is used, Contrast value is based on current 81H setting to increase or decrease. The contrast maximum value is 0xFF and minimum value is 0x00.

Example: up step 9, Pin[D7:D3]=[01001]



7.1.16. Set Segment Re-map: (A0H - A1H)

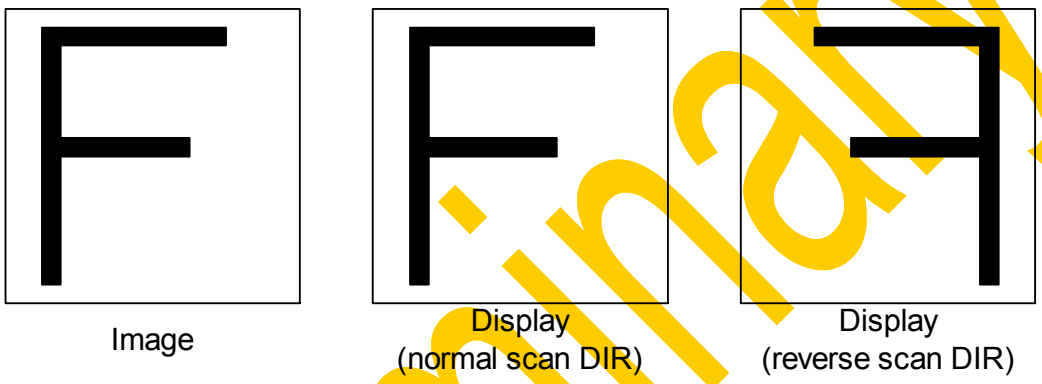
Change the relationship between RAM row address and segment driver. The order of segment driver output pads can be reversed by software. This allows flexible IC layout during OLED module assembly. For details, refer to the page address section of figure 23. When display data is written or read, the column address or page address (depends on the memory addressing mode) is incremented by 1 as shown in flowing figure

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R/$\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	0	0	ADC

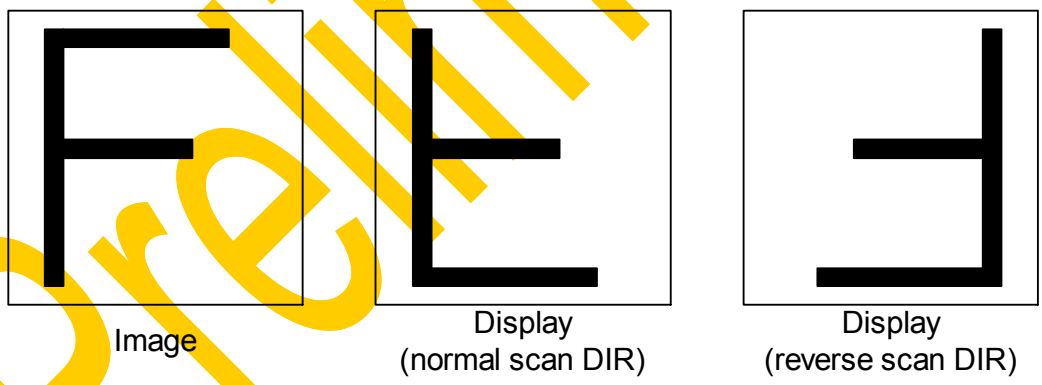
When ADC = “L”, the down rotates (normal direction). (default)

When ADC = “H”, the up rotates (reverse direction).

The display examples of Segment Re-map command are showed in flowing figure.



(a) ADC=0



(b) ADC=1(segment remap)

the display example of Set Segment Re-map and common scan direction command

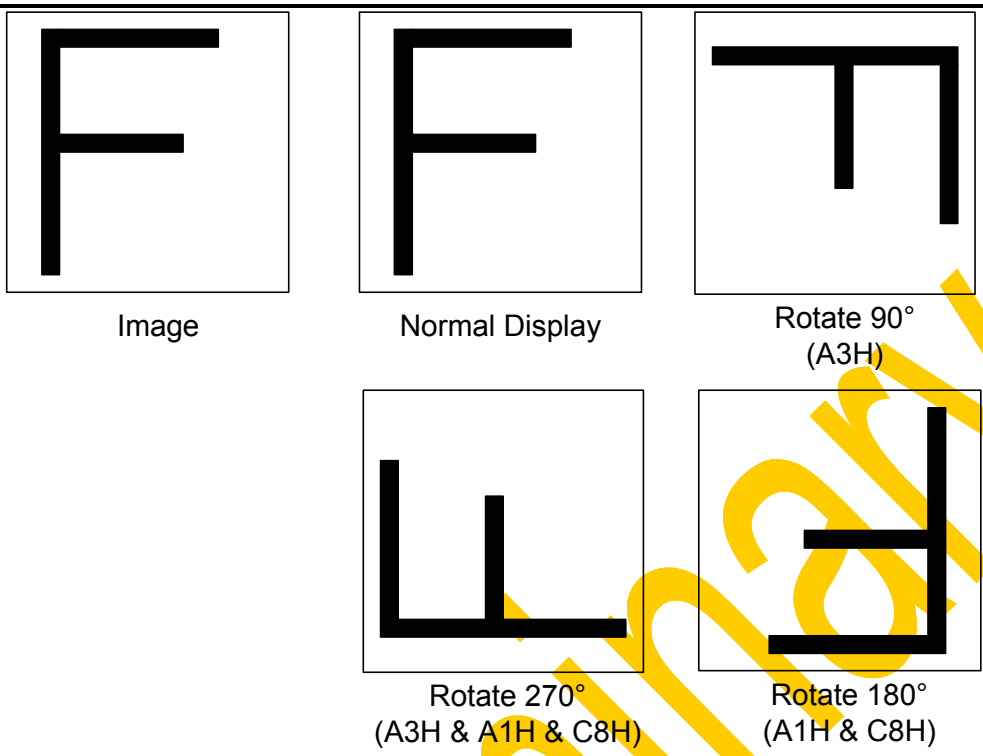
7.1.17. Set Display Rotation: (A3H)

Display can rotate 90 degrees. The rotate function work must in square resolution.

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R/$\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	0	1	1
0	1	0	*	*	*	*	*	*	*	D

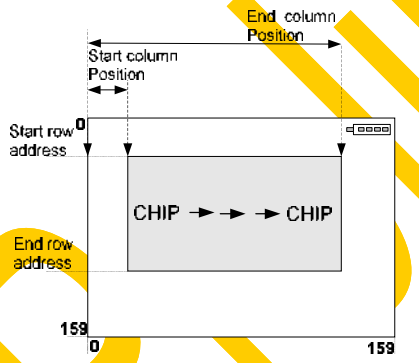
When D = “L”, Display doesn’t rotate (normal). (default)

When D = “H”, Display rotates 90°.

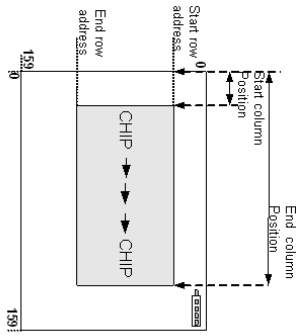


The display example of Set Ram rotation command

■ Rotate + Scrolling



Normal display + Horizontal scrolling



Rotate display + Horizontal scrolling

7.1.18. Set Entire Display OFF/ON: (A4H - A5H)

Forcibly turns the entire display on regardless of the contents of the display data RAM. At this time, the contents of the display data RAM are held.

This command has priority over the normal/reverse display command.

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R/$\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	1	0	D

When D = “L”, the normal display status is provided. (default)

When D = “H”, the entire display ON status is provided.

7.1.19. Set Normal/Reverse Display: (A6H -A7H)

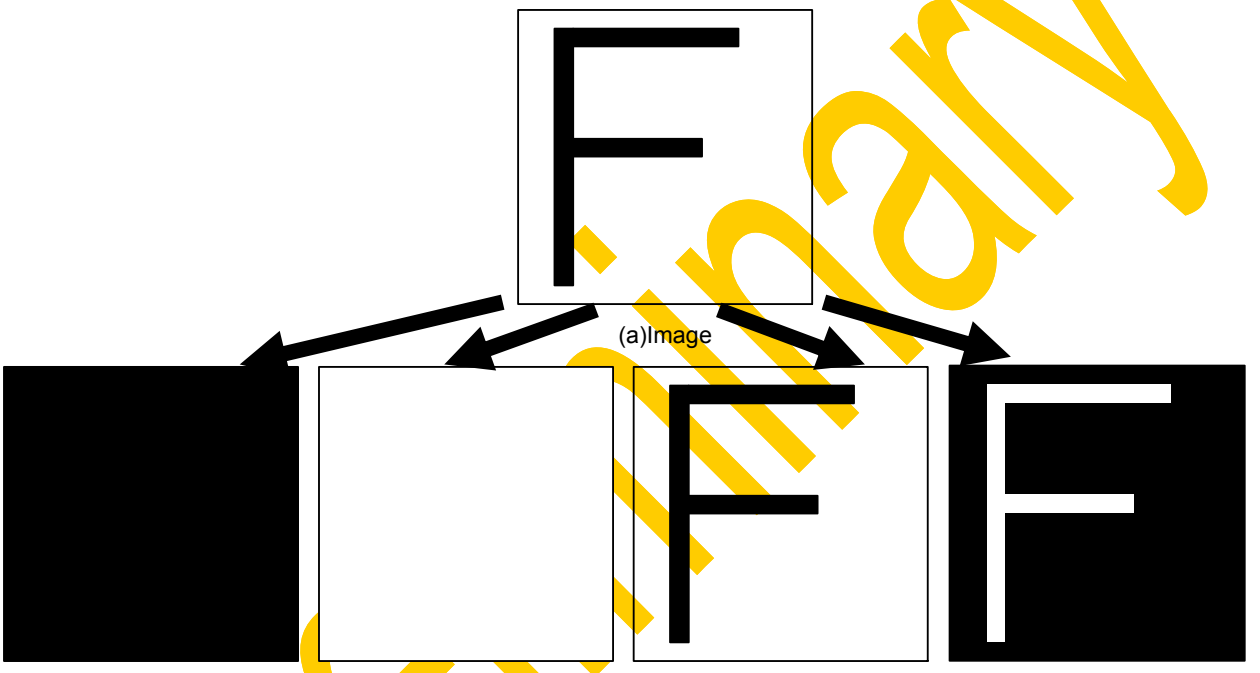
Reverse the display ON/OFF status without rewriting the contents of the display data RAM.

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R/$\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	1	1	D

When D = “L”, the RAM data is high, being OLED ON potential (normal display). (default)

When D = “H”, the RAM data is low, being OLED ON potential (reverse display)

The display example of Entire display off/on and normal/reverse command are showed in flowing figure.



(b) Display off (0xAE) (c) Entire display on (0xA5) (d) Normal display (0xA6) (e) Reverse display (0xA7)

Display example of entire display on and normal/reverse

7.1.20. Set Multiplex Ratio: (A8H) (Double Bytes Command)

This command switches default 160 multiplex modes to any multiplex ratio from 1 to 160. The output pads COM0-COM159 will be switched to corresponding common signal.

- Multiplex Ratio Mode Set: (A8H)

A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	0	0	0

- Multiplex Ratio Data Set: (00H – 9FH)

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R/$\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0	Multiplex Ratio

0	1	0	0	0	0	0	0	0	0	0	1
0	1	0	0	0	0	0	0	0	0	1	2
0	1	0	0	0	0	0	0	0	1	1	3
0	1	0					..				..
0	1	0	1	0	0	1	1	1	1	0	159
0	1	0	1	0	0	1	1	1	1	1	160(default)

7.1.21. Set Grayscale/Mono display mode: (ACH)

This command switches mono or gray mode.

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R/$\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	1	0	0
0	1	0	*	*	*	A4	*	*	A1	A0

When A0 = “L”, the grayscale display mode is provided. (default)

When A0 = “H”, the mono display mode is provided.

When A1 = “L”, In mono mode, the ram data bye format is composed of 8 seg data. (default)

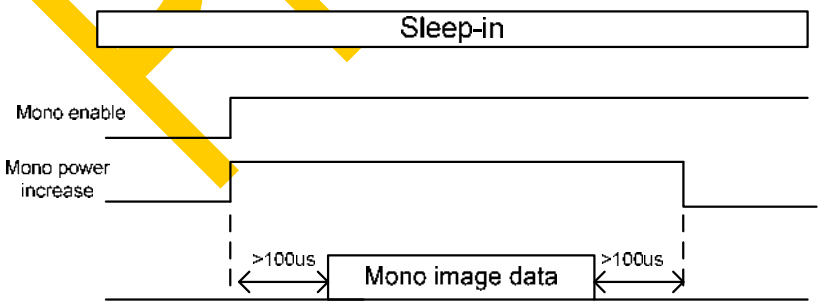
When A1 = “H”, In mono mode, the ram data bye format is composed of 8 com data.

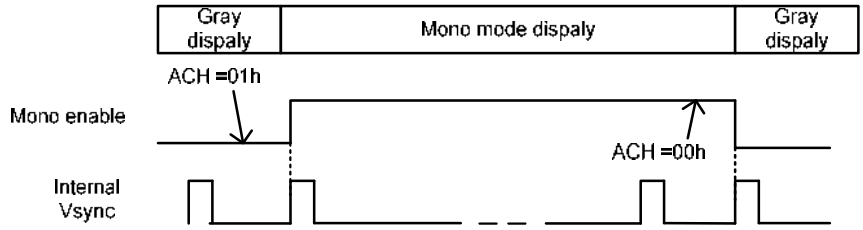
■ Mono power saving mode:

When mono mode enables, D = 0 is for writing mono image in sleep-in period. (Default)

When mono mode enables, D = 1 is for saving power in sleep-in period.

A0	A4	Driving mode in sleep-in period
0	0	Gray mode
0	1	Gray mode power increasing mode
1	0	Mono mode
1	1	Mono mode power increasing mode





Note. In mono mode, 21H Column end – Column start +1 must be even value

7.1.22. Display OFF/ON: (AEH - AFH)

Alternatively turns the display on and off.

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R/$\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	1	1	D

When D = “L”, Display OFF OLED. (default)

When D = “H”, Display ON OLED.

When the display OFF command is executed, power saver mode will be entered.

7.1.23. Set Gray Scale Table: (B8H) (Double Bytes Command)

This command is used to set each individual gray scale level for the display. Gray scale levels GS0 that has no pre-charge and current drive, each gray scale level is programmed in the length of current drive stage pulse width with unit of DCLK.

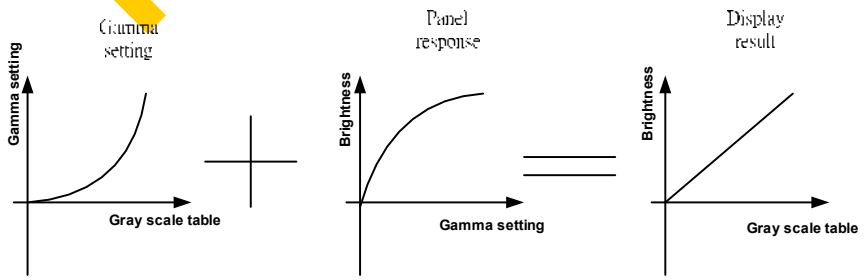
Following the command B8h, the user has to set the gray scale for GS1, GS2… GS14, GS15 one by one in sequence. The setting of gray scale table can perform gamma correction on panel display. Since the perception of the brightness scale shall match the image data value in display data RAM, appropriate gray scale table setting can compensate this effect.

- Gray Scale Table Setting: (B8H)

A0	$\overline{RD}$ (E)	R / $\overline{W}$ ($\overline{WR}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	1	1	0	0	0

- Gamma curve setting is 6 bits data format:

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R / $\overline{W}$)	D6	D5	D4	D3	D2	D1	D0	PWM-driving Default (hex)
0	1	0	GS0[6:0]							00
0	1	0	GS1[6:0]							01
0	1	0	GS2[6:0]							02
0	1	0	GS3[6:0]							03
0	1	0	GS4[6:0]							05
0	1	0	GS5[6:0]							08
0	1	0	GS6[6:0]							0C
0	1	0	GS7[6:0]							11
0	1	0	GS8[6:0]							17
0	1	0	GS9[6:0]							1E
0	1	0	GS10[6:0]							26
0	1	0	GS11[6:0]							2F
0	1	0	GS12[6:0]							39
0	1	0	GS13[6:0]							44
0	1	0	GS14[6:0]							50
0	1	0	GS15[6:0]							5E



Note : 1. The GS15 must larger than GS1~GS14.

2. The sum of GS15 and pre-charge and dis-charge must large than 0x65.

7.1.24. Set Linear Gray Scale Table Setting: (BAH)

This signal byte command is used to reloads linear gray scale level for the display GP0~15 is a default linear gray scale level.

RAM Data(4 bits)	Gamma Setting (Command B8h)	Default Gamma Setting for PWM-driving (Command BAh) (hex)
0000	GS0	00
0001	GS1	06
0010	GS2	0C
0011	GS3	12
0100	GS4	18
0101	GS5	1E
0110	GS6	24
0111	GS7	2A
1000	GS8	30
1001	GS9	36
1010	GS10	3C
1011	GS11	42
1100	GS12	48
1101	GS13	4E
1110	GS14	54
1111	GS15	5A

The example of gray scale compensate panel display

7.1.25. Set Common Output Scan Direction: (C0H – C8H)

This command sets the scan direction of the common output allowing layout flexibility in OLED module design. In addition, the display will have immediate effect once this command is issued. That is, if this command is sent during normal display, the graphic display will be vertically flipped.

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R/$\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
	1	0	1	1	0	0	D	*	*	*

When D = “L”, Scan from COM0 to COM [N -1]. (default)

When D = “H”, Scan from COM [N -1] to COM0.

7.1.26. Set Display Offset: (Double Bytes Command)

This is a double byte command. The next command specifies the mapping of display start line to one of COM0-159 (it is assumed that COM0 is the display start line, that equals to 0). For example, to move the COM16 towards the COM0 direction for 16 lines, the 6-bit data in the second byte should be given by 010000. To move in the opposite direction by 16 lines, the 6-bit data should be given by (160-16), so the second byte should be 10010000.

■ Display Offset Mode Set: (D3H)

A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0

0	1	0	1	1	0	1	0	0	1	1

■ Display Offset Data Set: (00H~9FH)

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R/$\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0	COMx
0	1	0	0	0	0	0	0	0	0	0	0(default)
0	1	0	0	0	0	0	0	0	0	1	1
0	1	0	0	0	0	0	0	0	1	1	2
0	1	0					..				..
0	1	0					..				..
0	1	0	1	0	0	1	1	1	1	0	158
0	1	0	1	0	0	1	1	1	1	1	159

Note: "*" stands for "Don't care"

COM pin	Multiplex ratio (A8) = 9Fh		Multiplex ratio (A8) = 7Fh	
	Display offset(D3H) =00h	Display offset(D3H) =0Ah	Display offset(D3H) =00h	Display offset(D3H) =0Ah
COM0	Row 0	Row 10	Row 0	Row 10
COM1	Row 1	Row 11	Row 1	Row 11
COM2	Row 2	Row 12	Row 2	Row 12
COM3	Row 3	Row 13	Row 3	Row 13
:	:	:	:	:
:	:	:	:	:
COM116	Row 116	Row 126	Row 116	Row 126
COM117	Row 117	Row 127	Row 117	Row 127
COM118	Row 118	Row 128	Row 118	-
COM119	Row 119	Row 129	Row 119	-
:	:	:	:	:
COM125	Row 125	Row 135	Row 125	-
COM126	Row 126	Row 136	Row 126	-
COM127	Row 127	Row 137	Row 127	-
COM128	Row 128	Row 138	-	-
COM129	Row 129	Row 139	-	-
COM130	Row 130	Row 140	-	-
:	:	:	:	:
COM146	Row 146	Row 156	-	-
COM147	Row 147	Row 157	-	-
COM148	Row 148	Row 158	-	-
COM149	Row 149	Row 159	-	-
COM150	Row 150	Row 0	-	Row 0
COM151	Row 151	Row 1	-	Row 1
:	:	:	:	:
COM156	Row 156	Row 6	-	Row 6
COM157	Row 157	Row 7	-	Row 7
COM158	Row 158	Row 8	-	Row 8
COM159	Row 159	Row 9	-	Row 9

Display offset COM output (C0H - COM0 to COM [N -1])

COM pin	Multiplex ratio (A8) = 9Fh		Multiplex ratio (A8) = 7Fh	
	Display offset(D3H) =00h	Display offset(D3H) =0Ah	Display offset(D3H) =00h	Display offset(D3H) =0Ah
COM0	Row 159	Row 9	Row 127	-
COM1	Row 158	Row 8	Row 126	-
COM2	Row 157	Row 7	Row 125	-
COM3	Row 156	Row 6	Row 124	-
:	:	:	:	:
COM8	Row 151	Row 1	Row 119	-
COM9	Row 150	Row 0	Row 118	-
COM10	Row 149	Row 159	Row 117	Row 127
COM11	Row 148	Row 158	Row 116	Row 126
COM12	Row 147	Row 157	Row 115	Row 125
COM13	Row 146	Row 156	Row 114	Row 124
:	:	:	:	:
:	:	:	:	:
COM116	Row 43	Row 53	Row 11	Row 21
COM117	Row 42	Row 52	Row 10	Row 20
COM118	Row 41	Row 51	Row 9	Row 19
COM119	Row 40	Row 50	Row 8	Row 18
:	:	:	:	:
COM125	Row 34	Row 44	Row 2	Row 12
COM126	Row 33	Row 43	Row 1	Row 11
COM127	Row 32	Row 42	Row 0	Row 10
COM128	Row 31	Row 41	-	Row 9
COM129	Row 30	Row 40	-	Row 8
COM130	Row 29	Row 39	-	Row 7
:	:	:	:	
COM135	Row 31	Row 41	-	Row 2
COM136	Row 30	Row 40	-	Row 1
COM137	Row 29	Row 39	-	Row 0
COM138	Row 30	Row 40	-	-
COM139	Row 29	Row 39	-	-
:	:	:	:	:
COM146	Row 13	Row 23	-	-
COM147	Row 12	Row 22	-	-
COM148	Row 11	Row 21	-	-
COM149	Row 10	Row 20	-	-
COM150	Row 9	Row 19	-	-
COM151	Row 8	Row 18	-	-
:	:	:	:	:
COM156	Row 3	Row 13	-	-
COM157	Row 2	Row 12	-	-
COM158	Row 1	Row 11	-	-
COM159	Row 0	Row 10	-	-

Display offset COM output (C8H - COM [N -1] to COM0)

7.1.27. Set Display Clock Divide Ratio/Oscillator Frequency: (Double Bytes Command)

This command is used to set the frequency of the internal display clocks (DCLKs). It is defined as the divide ratio used to divide the oscillator frequency. Frame frequency is determined by divide ratio, number of display clocks per row, MUX ratio and oscillator frequency.

- Divide Ratio/Oscillator Frequency Mode Set: (D5H)

A0	E / RD	R / W / WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	1	0	1	0	1

- Divide Ratio/Oscillator Frequency Data Set: (00H - FFH)

A0	E / RD	R / W / WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	A7	A6	A5	A4	A3	A2	A1	A0

- A7 – A5 defines the divide ration of the display clocks (DCLK).

A7	A6	A5	Divide Ratio
0	0	0	2(default)
0	0	1	4
0	1	0	6
0	1	1	8
1	0	0	10
1	0	1	12
1	1	0	14
1	1	1	15

- A4 – A0 sets the oscillator frequency. Oscillator frequency increase with the value of A[4:0] and vice versa.

A4	A3	A2	A1	A0	Oscillator Frequency of fOSC
0	0	0	0	0	+0% (default)
0	0	0	0	1	+1.85%
0	0	0	1	0	+3.65%
0	0	0	1	1	+5.45%
0	0	1	0	0	+7.25%
0	0	1	0	1	+8.95%
0	0	1	1	0	+10.65%
0	0	1	1	1	+12.35%
0	1	0	0	0	+13.95%
0	1	0	0	1	+15.50%
0	1	0	1	0	+17.05%
0	1	0	1	1	+18.60%
0	1	1	0	0	+20.15%
0	1	1	0	1	+21.70%
0	1	1	1	0	+23.25%
0	1	1	1	1	+24.75%
1	0	0	0	0	-2.10%

1	0	0	0	1	-3.95%
1	0	0	1	0	-5.80%
1	0	0	1	1	-7.70%
1	0	1	0	0	-9.65%
1	0	1	0	1	-11.60%
1	0	1	1	0	-13.60%
1	0	1	1	1	-15.60%
1	1	0	0	0	-17.60%
1	1	0	0	1	-19.60%
1	1	0	1	0	-21.70%
1	1	0	1	1	-23.80%
1	1	1	0	0	-26.00%
1	1	1	0	1	-28.20%
1	1	1	1	0	-30.40%
1	1	1	1	1	-32.60%

7.1.28. Set Discharge_front Period (93H): (Two Bytes Command)

This command is used to set the duration of the discharge period. The interval is counted in number of DCLK.

- Discharge_front Period Mode Set: (93H)

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R/$\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	1	0	0	1	1
0	1	0	0	0	0	A_4	A_3	A_2	A_1	A_0

- Discharge_front Period Adjust : (A4 - A0)

A_4	A_3	A_2	A_1	A_0	Discharge_front
0	0	0	0	0	N.A
0	0	0	0	1	1 DCLK
0	0	0	1	0	2 DCLK
:	:	:	:	:	:
1	1	0	1	0	26 DCLK(Default)
:	:	:	:	:	:
1	1	1	1	1	31 DCLK

7.1.29. Set Discharge_back Period (D8H): (Two Bytes Command)

This command is used to set the duration of the discharge period. The interval is counted in number of DCLK.

- Discharge_back Period Mode Set: (D8H)

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R/$\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	1	1	0	0	0
0	1	0	0	0	0	A_4	A_3	A_2	A_1	A_0

■ Discharge_back Period Adjust : (A4 - A0)

A_4	A_3	A_2	A_1	A_0	Discharge_back
0	0	0	0	0	0 DCLK
0	0	0	0	1	1 DCLK
0	0	0	1	0	2 DCLK (Default)
0	:	:	:	:	:
1	1	1	1	0	30 DCLK
1	1	1	1	1	31 DCLK

7.1.30. Set Pre-charge Period (D9H): (Two Bytes Command)

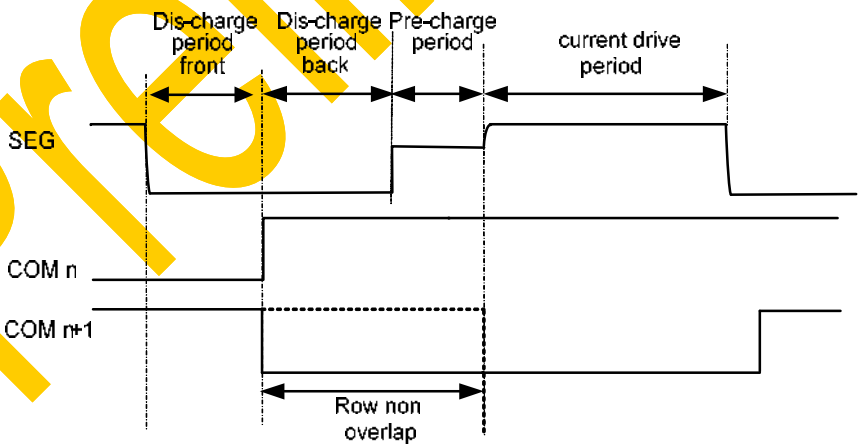
This command is used to set the duration of the pre-charge period. The interval is counted in number of DCLK. DEFAULT is 2 DCLKs.

■ Pre-charge Period Mode Set: (D9H)

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R/$\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	1	1	0	0	1
0	1	0	0	0	0	A_4	A_3	A_2	A_1	A_0

■ Pre-charge Period Adjust : (A4 - A0)

A_4	A_3	A_2	A_1	A_0	Pre-charge Period
0	0	0	0	0	0 DCLK
0	0	0	0	1	1 DCLK
0	0	0	1	0	2 DCLK (Default)
0	:	:	:	:	:
1	1	1	1	0	30 DCLK
1	1	1	1	1	31 DCLK



7.1.31. Set SEG pads hardware configuration: (DAH) (Double Bytes Command)

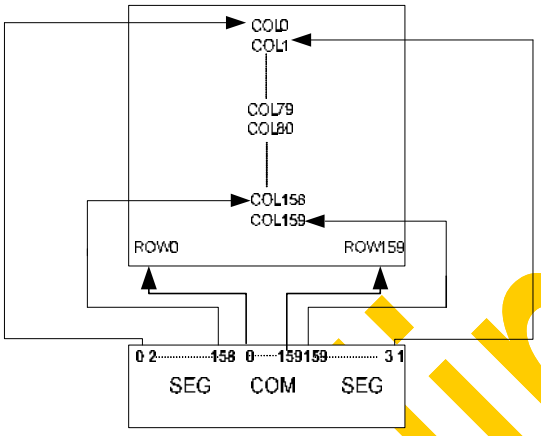
This command is to set the SEG signals pad configuration to match the OLED panel hardware layout.

■ SEG Pads Hardware Configuration Mode Set: (DAH)

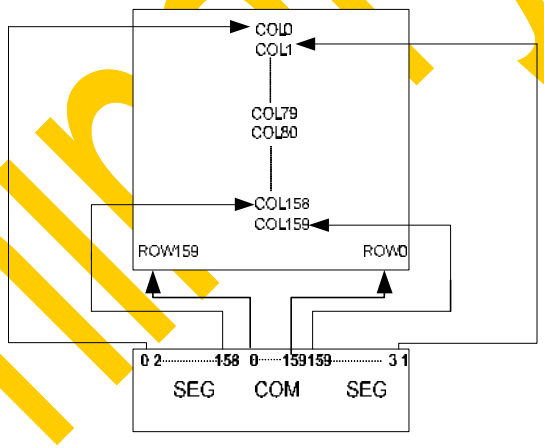
A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	1	1	0	1	0
0	1	0	0	0	0	0	0	0	A1	A0

When A0 = “L”, Even on the left. (default)
When A0 = “H”, Even on the right.
When A1 = “L”, Alternative. (default)
When A1 = “H”, Sequential.

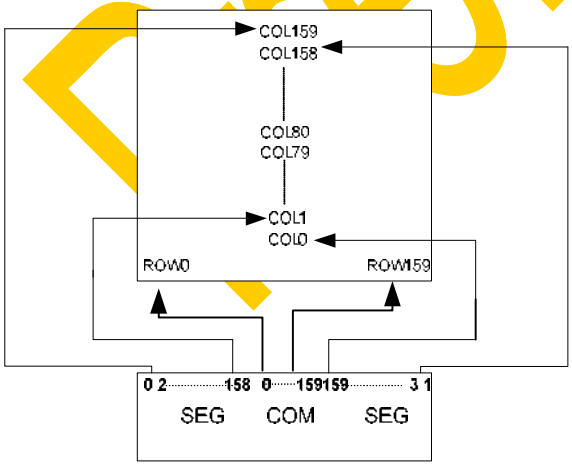
Please see the following figure for Set Segment Re-map and SEG pads hardware configuration.



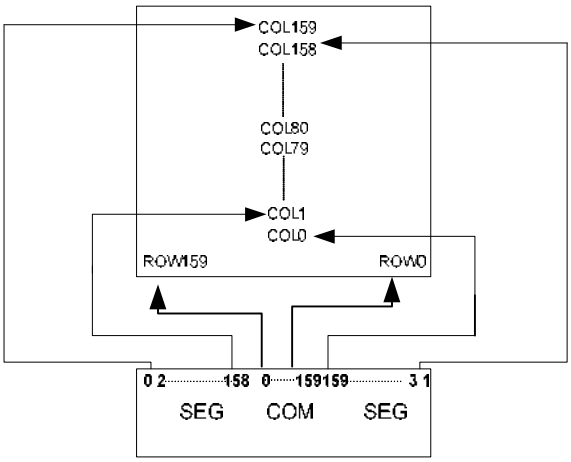
(1) DAH=00 , A0H(SEG0 to SEG159),
C0H(COM0 to COM[N-1])



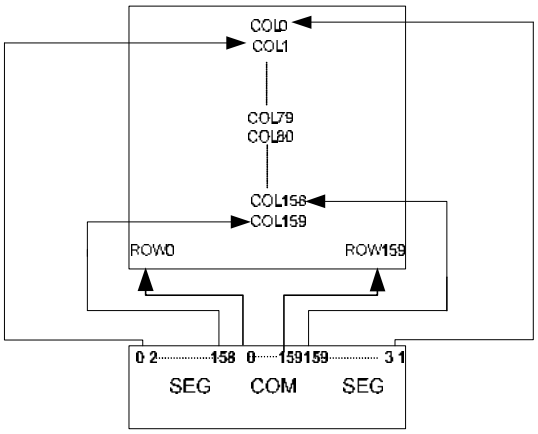
(2) DAH=00 , A0H(SEG0 to SEG159),
C8H(COM[N-1] to COM0)



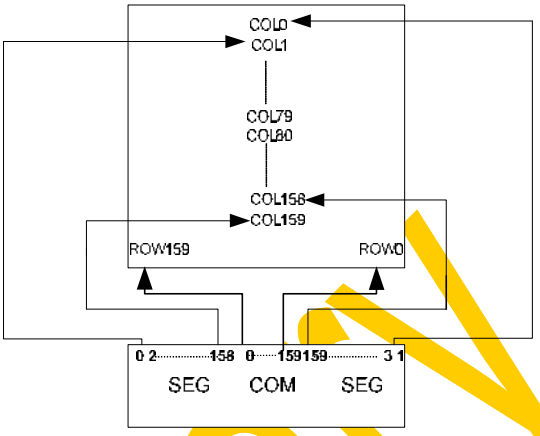
(3) DAH=00 , A1H(SEG159 to SEG0),
C0H(COM0 to COM[N-1])



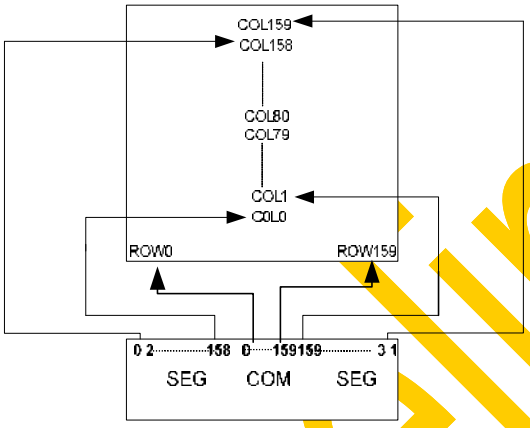
(4) DAH=00 , A1H(SEG159 to SEG0),
C8H(COM[N-1] to COM0)



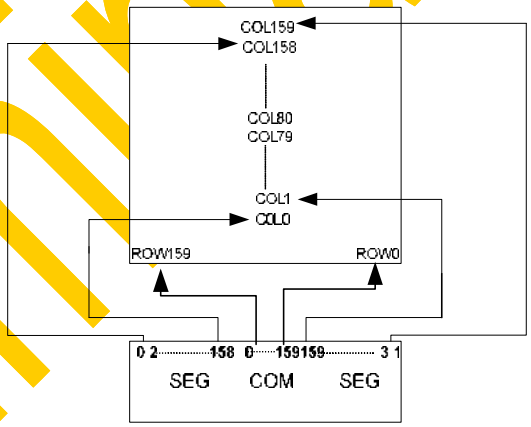
(5) DAH=01 , A0H(SEG0 to SEG159),
C0H(COM0 to COM[N-1])



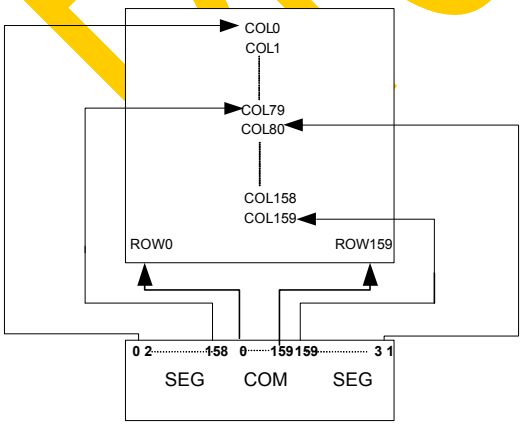
(6) DAH=01 , A0H(SEG0 to SEG159),
C8H(COM[N-1] to COM0)



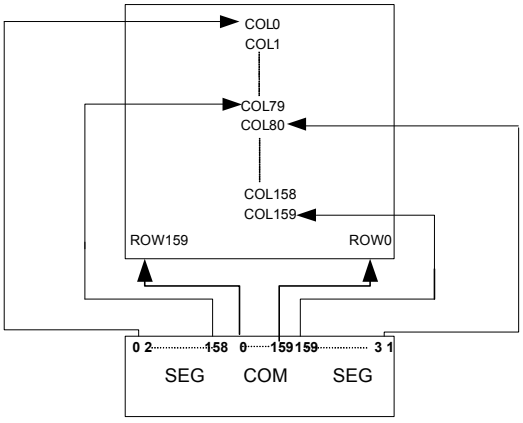
(7) DAH=01 , A1H(SEG159 to SEG0),
C0H(COM0 to COM[N-1])



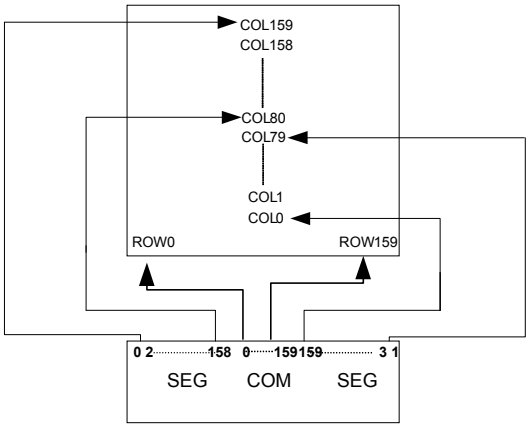
(8) DAH=01 , A1H(SEG159 to SEG0),
C8H(COM[N-1] to COM0)



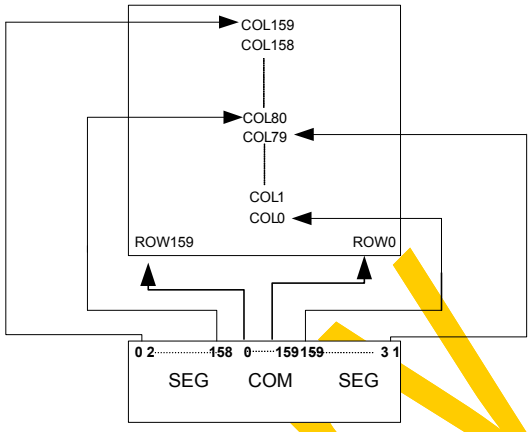
(9) DAH=10 , A0H(SEG0 to SEG159),
C0H(COM0 to COM[N-1])



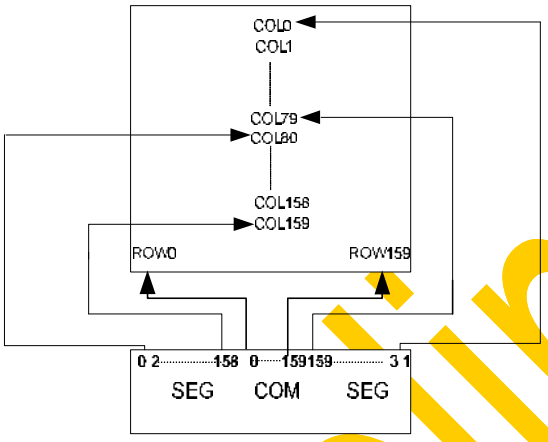
(10) DAH=10 , A0H(SEG0 to SEG159),
C8H(COM[N-1] to COM0)



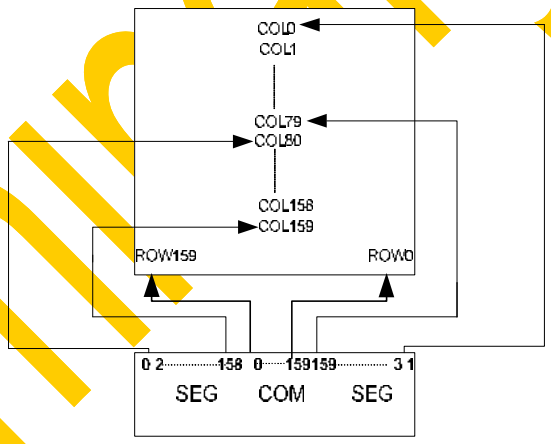
(11) DAH=10 , A1H(SEG159 to SEG0),
C0H(COM0 to COM[N-1])



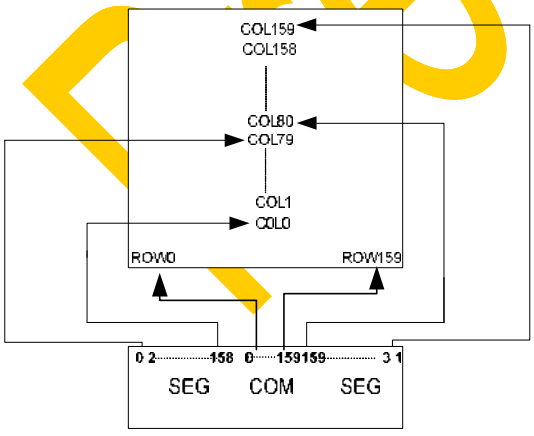
(12) DAH=10 , A1H(SEG159 to SEG0),
C8H(COM[N-1] to COM0)



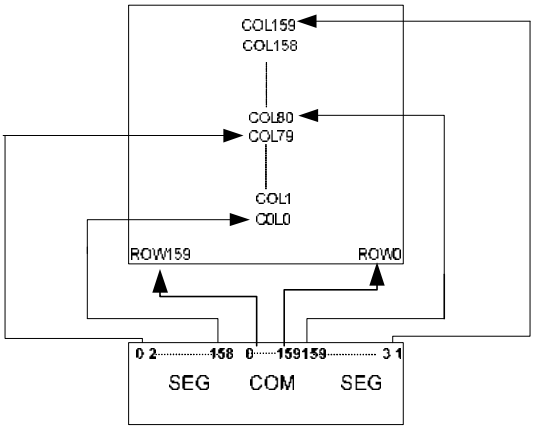
(13) DAH=11 , A0H(SEG0 to SEG159),
C0H(COM0 to COM[N-1])



(14) DAH=11 , A0H(SEG0 to SEG159),
C8H(COM[N-1] to COM0)



(15) DAH=11 , A1H(SEG159 to SEG0),
C0H(COM0 to COM[N-1])



(16) DAH=11 , A1H(SEG159 to SEG0),
C8H(COM[N-1] to COM0)

SEG pads hardware configuration

7.1.32. Set VCOM Deselect Level: (DBH) (Double Bytes Command)

This command is to set the common pad output voltage level at deselect stage.

VCOM Deselect Level Mode Set: (DBH)

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	1	1	0	1	1

VCOM Deselect Level Data Set: (00H - FFH)

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0

VCOMH = β1 X VREF = (0.430 + A [7:0] X 0.006415) X VREF

A[7:0]	β_1	A[7:0]	β_1
00H	0	20H	0.635
01H	0.436	21H	0.642
02H	0.442	22H	0.648
03H	0.449	23H	0.654
04H	0.456	24H	0.661
05H	0.462	25H	0.667
06H	0.468	26H	0.674
07H	0.475	27H	0.680
08H	0.481	28H	0.687
09H	0.488	29H	0.693
0AH	0.494	2AH	0.699
0BH	0.501	2BH	0.706
0CH	0.507	2CH	0.712
0DH	0.513	2DH	0.719
0EH	0.520	2EH	0.725
0FH	0.526	2FH	0.731
10H	0.533	30H	0.738
11H	0.539	31H	0.744
12H	0.546	32H	0.751
13H	0.552	33H	0.757
14H	0.558	34H	0.764
15H	0.565	35H	0.770
16H	0.571	36H	0.776
17H	0.578	37H	0.783
18H	0.584	38H	0.789
19H	0.590	39H	0.796
1AH	0.596	3AH	0.802
1BH	0.603	3BH	0.808
1CH	0.610	3CH	0.815
1DH	0.616	3DH	0.821
1EH	0.622	3EH	0.828
1FH	0.629	3FH	0.834 (default)
40H - FFH	1		

Note. VREF = VPP

7.1.33. Set Row non- overlap: (DCH) (Double Bytes Command).

This command is used to set the duration of the row non-overlap period.

Row non-overlap Set: (DCH)

A0	E / $\overline{RD}$	R / $\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	1	1	1	0	0

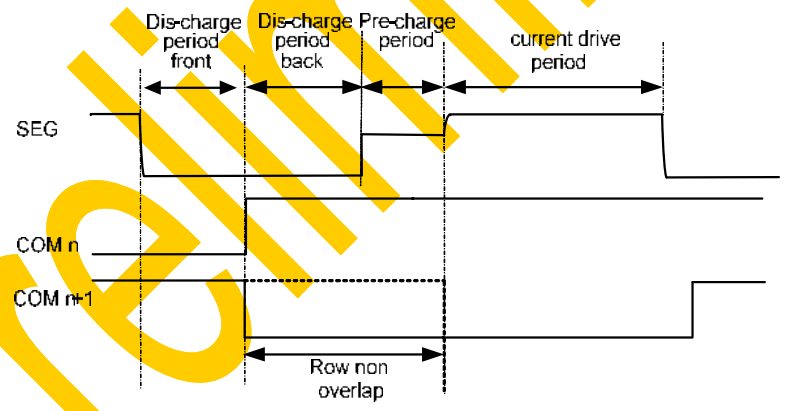
Row non-overlap /SEG Hiz Period Data Set: (00H – 7FH)

A0	E / $\overline{RD}$	R / $\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	A_6	A_5	A_4	A_3	A_2	A_1	A_0

Row non-overlap Period Adjust: (A7 - A0)

A_6	A_5	A_4	A_3	A_2	A_1	A_0	Row non-overlap Period
0	0	0	0	0	0	0	1 DCLK(default)
0	0	0	0	0	0	1	2 DCLKs
0	0	0	0	0	1	0	3 DCLKs
:	:	:	:	:	:	:	:
1	0	1	1	1	1	0	95 DCLKs
1	0	1	1	1	1	1	96 DCLKs

Please see the following figure for Dis-charge/Pre-charge/Row non-overlap.



Note: The time between COM n rising and COM n-1 falling is 1 DCLK.

7.1.34. Pre-charge VSEGH Level control (DDH):

A0	E / $\overline{RD}$	R / $\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	1	1	1	0	1
0	1	0	*	*	*	A4	A3	A2	A1	A0

- VSEGH level control: (A4 - A0)

VSEGH[4:0] : VSEGH = N x Vpp

VSEGH[4:0]	N
0	0.1
1	0.125
2	0.15
…	…
10	0.35
11	0.375
12	0.4
13	0.425
14	0.45
15	0.475(Default)
16	0.5
17	0.525
…	…
29	0.825
30	N.A.
31	N.A.

7.1.35. Read-Modify-Write: (E0H)

A pair of Read-Modify-Write and End commands must always be used. In page addressing mode, once read-modify-write is issued, column address is not incremental by read display data command but incremental by write display data command only. In vertical addressing mode, once read-modify-write is issued, page address is not incremental by read display data command but incremental by write display data command only. It continues until End command is issued. When the End is issued, column address or page address (it depends on the addressing mode) returns to the address when read-modify-write is issued. This can reduce the microprocessor load when data of a specific display area is repeatedly changed during cursor blinking or others.

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R/$\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	0	0

Cursor display sequence:

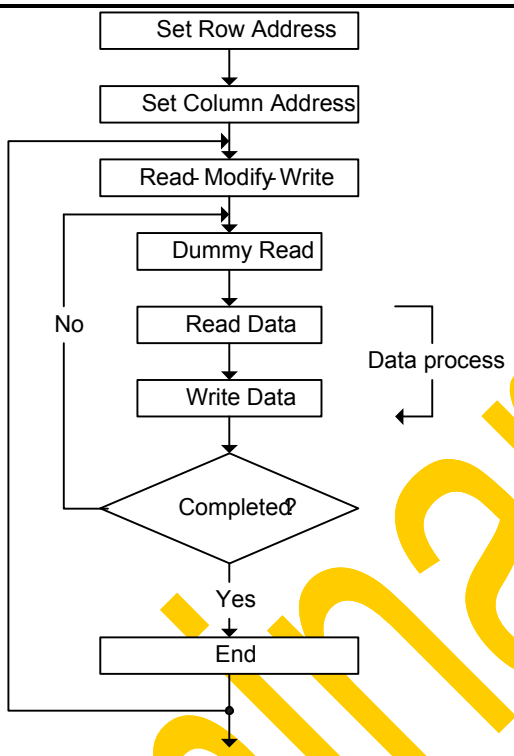


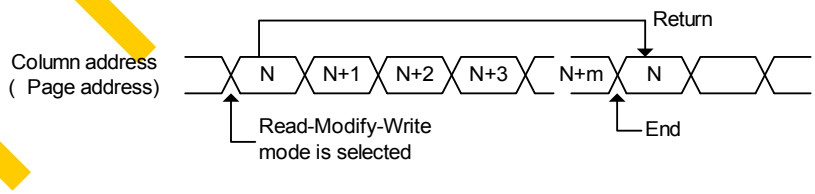
Figure 28

Note. The size of data to write or read per time is one byte. This function only support in 8080/6800 interfaces, and does not support in 1-bit mono mode.

7.1.36. End: (EEH)

Cancels Read-Modify-Write mode and returns column address or page address (it depends on the RAM addressing mode) to the original address (when Read-Modify-Write is issued.)

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R/$\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	1	0



7.1.37. NOP: (E3H)

No Operation Command.

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R/$\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	1

7.1.38. Write Display Data

Write 8-bit data in display RAM. As the column address is incremental by 1 automatically after each write, the microprocessor can continue to write data of multiple words.

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R/$\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	Write RAM data							

7.1.39. Read Status

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R/$\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	BUSY	ON/OFF	ID					

BUSY: When high, the CH1120 is busy due to internal operation or reset.

ON/OFF: Indicates whether the display is on or off. When it goes low, the display turns on. When it goes high, the display turns off. This is the opposite of Display ON/OFF command.

ID： These bits contain the information of the chip. The output bits 100000(it means CH1120).

Note: D/$\overline{C}$ or A0 must be set to low before reading status.

7.1.40. Read Display Data

Reads 8-bit data from display RAM area specified by column address and page address. As the column address or page address (depends on the mode of memory addressing) is increment by 1 automatically after each write, the microprocessor can continue to read data of multiple words. A single dummy read is required immediately after column address being setup. Refer to the display RAM section of FUNCTIONAL DESCRIPTION for details. Note that no display data can be read via the serial interface.

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R/$\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	Read RAM data							

Note:CH1120 doesn't support read sram in Mono mode.

7.1.41. Read Panel ID (only-read): (E1H)

This command is to read Panel ID by hardware pin ID0&ID1 setting.

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R/$\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	1	1	0	0	0	0	1
1	0	1	0	0	0	0	0	0	ID1	ID0

7.1.42. Set CMD Protection: (FDH)

This command is used to prohibit the command access to avoid the noise until to disable this function.

CMD Protection Set: (FDH)

A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	1	1	1	0	1
0	1	0	0	0	1	0	1	0	1	0
0	1	0	0	1	0	1	0	0	1	0

When sending [2Ah (Key1) , 52h(Key2)], it means to disable the protection.

When sending others, it means to enable the protection.

7.1.43. DVDD Regulator Off CMD (99H)

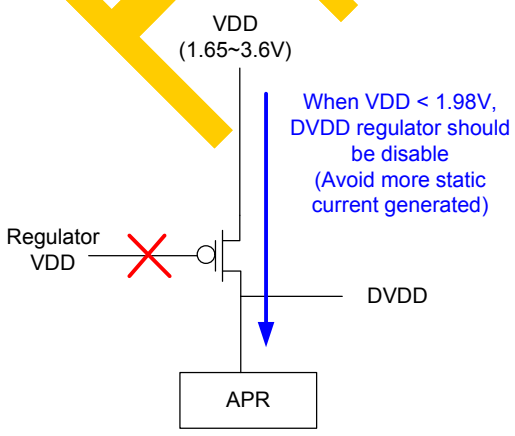
When VDD <1.98V & DVDD_EN pin is high, writing this CMD to turn off the DVDD regulator circuit for avoiding more static current generated on VDD.

A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	1	1	0	0	1
0	1	0	DVDD_REG_EN1[7:0]							
0	1	0	DVDD_REG_EN2[7:0]							
0	1	0	DVDD_REG_EN3[7:0]							

When power on, DVDD regulator is enable. (default)
When DVDD_REG_EN1 [7:0] = 5A & DVDD_REG_EN2 [7:0] = A5 & DVDD_REG_EN3 [7:0] = AA, DVDD regulator is disable. When DVDD_REG_EN1 [7:0], DVDD_REG_EN2 [7:0]. DVDD_REG_EN3 [7:0] are other value, DVDD regulator is enable. The relation between DVDD_EN hardware pin and DVDD regulator off command is as below:

(Between “Hardware pin” and “Command” are a logic AND function.)

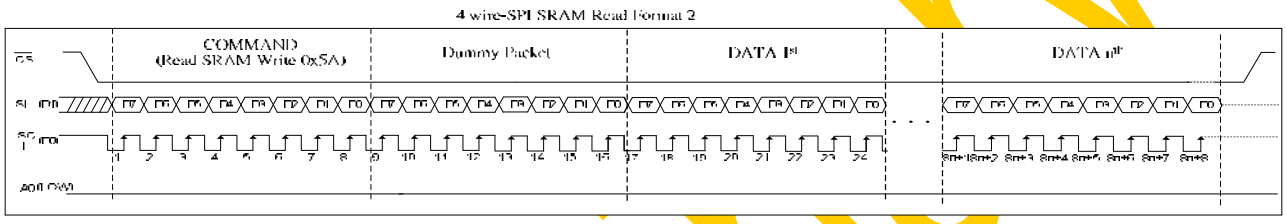
DVDD_ EN Hardware pin	DVDD regulator off Command	Result
1	0 (5A.A5.AA)	0 (Regulator OFF)
1	1 (default)	1 (Regulator ON)



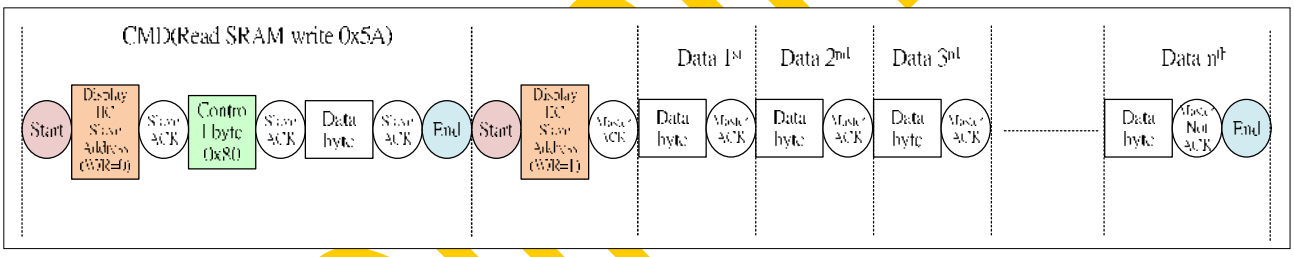
7.1.44. SRAM read cmd in SPI&I2C (5AH)

A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	1	0	1	1	0	1	0
0	1	0	rd_sram_data							

Ex:



I2C read sram



7.1.45. Set RAM power : (DEH)

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R/$\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	1	1	1	1	0
0	1	0	*	*	*	A4	*	*	*	A0

When A0 = 1 , it means to enable SRAM 1st power. (Default)

When A4 = 1 , it means to enable SRAM 2nd power.(Default)

If user needs to save the RAM power in sleep in mode, set A0 = 0 and A4 = 0. If setting A0 & A4 =0 in sleep-in mode, user have to enable 1st power first then 2nd power

7.1.46. SPI_read data output mode (92H)

A0	E / $\overline{RD}$	R / $\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	1	0	0	1	0
0	1	0	spi_dout_sel[7:0]							

Note2: When Serial Interface (SPI) is selected, data output to data pin D1 or D2 in read cmd or ram.

spi_dout_sel[7:0] = 0x00 (or not 0x69) , SPI data output to data pin D1. (default)

spi_dout_sel[7:0] = 0x69, SPI data output to data pin D2.

7.1.47. Read IC ID (only-read): (E2H)

This command is used to read IC ID (This content is the same as Read Status). The default value is 0x60.

.

A0	$\overline{RD}$ (E)	$\overline{WR}$ (R / $\overline{W}$)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	1	1	0	0	0	1	0
1	0	1	BUSY	ON/OFF	IC ID					

BUSY: When high, the CH1120 is busy due to internal operation or reset.

ON/OFF: Indicates whether the display is on or off. When it goes low, the display turns on. When it goes high, the display turns off. This is the opposite of Display ON/OFF command.

IC ID： These bits contain the information of the chip. The output bits 100000(it means CH1120).

8. Command Table

Command	Code											Function
	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
1. Set Lower Column Start Address (00H-0FH)	0	1	0	0	0	0	0	Lower column start address				Sets 4 lower bits of column start address of display RAM in register. (DEFAULT = 00H)
2.Set Higher Column Start Address (10H-14H)	0	1	0	0	0	0	1	0	Higher column start address			Sets 4 higher bits of column start address of display RAM in register. (DEFAULT = 10H)
3. Set Row Start Address of Display RAM (B0H)	0	1	0	1	0	1	1	0	0	0	0	Specify Row address to load display RAM data to Row address register. (DEFAULT=00H)
	0	1	0	Row start address								
4. Set Column Start/End Address of Display RAM (21H)	0	1	0	0	0	1	0	0	0	0	1	Specifies column start/end address to load display RAM data to row address register. (Start address DEFAULT = 00H, END address DEFAULT = 4FH)
	0	1	0	0	Column start address							
	0	1	0	0	Column end address							
5. Set Row Start/End Address of Display RAM (22H)	0	1	0	0	0	1	0	0	0	1	0	Specifies row start/end address to load display RAM data to row address register. (Start address DEFAULT = 00H, END address DEFAULT = 9FH)
	0	1	0	Row start address								
	0	1	0	Row end address								
6.Set memory addressing mode (20H)	0	1	0	0	0	1	0	0	0	0	0	D = 1, Vertical Addressing Mode D = 0, Horizontal Addressing Mode (DEFAULT=00H)
	0	1	0	*	*	*	*	*	*	*	D	
7. Set Breathing Light (23H)	0	1	0	0	0	1	0	0	0	1	1	This command set Breathing Light ON/OFF and Time Interval. (DEFAULT=01H, 01H)
	0	1	0	ON/OFF	bre_test	*	A4	A3	A2	A1	A0	
	0	1	0	0	C2	C1	C0	0	B2	B1	B0	
8. Horizontal Scroll & Vertical Scroll Setup (24H-27H)	0	1	0	0	0	1	0	0	1	D1	D0	This command determined the scrolling direction (DEFAULT=26H) and the scrolling start column (DEFAULT=00H), end column (DEFAULT=9FH), start row (DEFAULT=00H), end row (DEFAULT=9FH) position and time interval(DEFAULT=00H). Before issuing this command, the horizontal/vertical scroll must be deactivated (2EH).
	0	1	0	A7	A6	A5	A4	A3	A2	A1	A0	
	0	1	0	B7	B6	B5	B4	B3	B2	B1	B0	
	0	1	0	C7	C6	C5	C4	C3	C2	C1	C0	
	0	1	0	D7	D6	D5	D4	D3	D2	D1	D0	
	0	1	0	*	*	*	*	*	E2	E1	E0	

9. Set Scroll Mode (28H-2BH)	0	1	0	0	0	1	0	1	0	D1	D0	Control continuous/single screen scroll and the way of writing all ram data or 1 column/row ram data for scrolling (DEFAULT=28H)
10. 1 Column/Row scroll mode display scroll (EBH)	0	1	0	1	1	1	0	1	0	1	1	This command is to scroll display in 1 column/row scroll mode.
	0	1	0	*	*	*	*	*	*	*	D	
11. Set Deactivate /Activate Horizontal Scroll(2EH-2FH)	0	1	0	0	0	1	0	1	1	1	D	This command is to Stop or start motion of horizontal/vertical scrolling. (DEFAULT=2EH)
12. Partial Display Setup (2CH-2DH)	0	1	0	0	0	1	0	1	1	0	D	This command consists of 6 consecutive bytes to set up the display area in column start/end address and row start/end address. When D=1(CMD 2DH), the partial display mode is enable.
	0	1	0	A7	A6	A5	A4	A3	A2	A1	A0	
	0	1	0	B7	B6	B5	B4	B3	B2	B1	B0	
	0	1	0	C7	C6	C5	C4	C3	C2	C1	C0	
	0	1	0	D7	D6	D5	D4	D3	D2	D1	D0	
13. Set Display Start Line(A2H)	0	1	0	1	0	1	0	0	0	1	0	Specifies line address to determine the initial display line or COM0.(DEFAULT=00H)
	0	1	0	Display Start line Set								
14. The Contrast Control Mode Set	0	1	0	1	0	0	0	0	0	0	1	This command is to set Contrast Setting of the display. The chip has 256 contrast steps from 00 to FF. (DEFAULT = 80H)
Contrast Data Register Set(81H)	0	1	0	Contrast Data								
15. External or internal IREF Set(ADH)	0	1	0	1	0	0	0	0	0	1	0	IREF can be controlled by external resister or internal resister.(DEFAULT=02H)
	0	1	0	MS_SEL	CMD_MODE	*	*	iseg_hw_adj_en	D2	D1	D0	
16. Set Segment Re-map (ADC) (A0H-A1H)	0	1	0	1	0	1	0	0	0	0	ADC	The down (0) or up (1) rotation. (DEFAULT = A0H)
17. Set Display Rotation (A3H)	0	1	0	1	0	1	0	0	0	1	1	The normal (0) or 90° (1) rotation. (DEFAULT = 00H)
	0	1	0	*	*	*	*	*	*	*	D	
18. Set Entire Display OFF/ON(A4H-A5H)	0	1	0	1	0	1	0	0	1	0	D	Selects normal display (0) or Entire Display ON (1). (DEFAULT = A4H)
19. Set Normal/ Reverse Display (A6H-A7H)	0	1	0	1	0	1	0	0	1	1	D	Normal indication (0) when low, but reverse indication (1) when high. (DEFAULT = A6H)
20. Set Multiplex Ratio	0	1	0	1	0	1	0	1	0	0	0	This command switches

(A8H)	0	1	0	Resolution set									default 160 multiplex modes to any multiplex ratio from 1 to160.(DEFAULT=9FH)
21. Set Grayscale/ Mono display mode (ACH)	0	1	0	1	0	1	0	1	1	0	0		Grayscale display mode (D=0) or Mono display mode (D=1). (DEFAULT = 00H)
	0	1	0	*	*	*	A4	*	*	A1	A0		
22. Display OFF/ON (AEH-AFH)	0	1	0	1	0	1	0	1	1	1	D		Turns on OLED panel (1) or turns off (0). (DEFAULT = AEH)
23. Set Gray Scale Table(B8H)	0	1	0	1	0	1	1	1	0	0	0		Set Gray Scale Table (DEFAULT = 00H,01H,02H,03H,05H,08H, 0CH,11H,17H,1EH,26H,2FH, 39H,44H,50H,5EH)
				GS0 [7]	GS0 [6]	GS0 [5]	GS0 [4]	GS0 [3]	GS0 [2]	GS0 [1]	GS0 [0]		

				GS15 [7]	GS15 [6]	GS15 [5]	GS15 [4]	GS15 [3]	GS15 [2]	GS15 [1]	GS15 [0]		
24. Set Default Linear Gray Scale Table for PWM-driving mode (BAH)	0	1	0	1	0	1	1	1	0	1	0		Set Default Linear Gray Scale Table for PWM-driving mode
25. Set Common Output Scan Direction (C8H)	0	1	0	1	1	0	0	D	*	*	*		Scan from COM0 to COM [N – 1] (0) or Scan from COM [N -1] to COM0 (1). (DEFAULT = C0H)
26. Set Display Offset (D3H)	0	1	0	1	1	0	1	0	0	1	1		The next command specifies the mapping of display start line to one of COM0-159. (DEFAULT=00H)
	0	1	0	Display Offset Data Set									
27. Set Display Divide Ratio/Oscillator Frequency Mode Set (D5H)	0	1	0	1	1	0	1	0	1	0	1		This command is used to set the frequency of the internal display clocks. (DEFAULT = 00H)
	0	1	0	Divide Ratio			Oscillator Frequency						
28. Set Dis-charge Period (93H)	0	1	0	1	0	0	1	0	0	1	1		This command is used to set the duration of the dis-charge period. (DEFAULT = 1AH)
				*	*	*	Dis-charge Period						
29. Set Dis-charge Period (D8H)	0	1	0	1	1	0	1	1	0	0	0		This command is used to set the duration of the pre-charge and dis-charge period. (DEFAULT = 02H)
				*	*	*	Dis-charge Period						
30. Set Pre-charge Period (D9H)	0	1	0	1	1	0	1	1	0	0	1		This command is used to set the duration of the pre-charge period. (DEFAULT = 02H)
				*	*	*	*	Pre-charge Period					

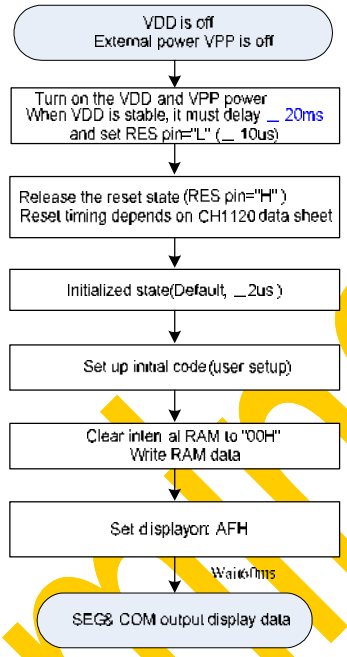
31. Set SEG pads hardware configuration (DAH)	0	1	0	1	1	0	1	1	0	1	0	This command is to set the SEG signals pad configuration to match the OLED panel hardware layout. (DEFAULT = 00H)
	0	1	0	*	*	*	*	*	*	A1	A0	
32. VCOM Deselect Level (DBH)	0	1	0	1	1	0	1	1	0	1	1	This command is to set the common pad output voltage level at deselect stage. (DEFAULT = 3FH)
	0	1	0	VCOM = (β_1 X V_{REF})								
33. Set Row non-overlap/SEG Pre_Dis-charge Period (DCH)	0	1	0	1	1	0	1	1	1	0	0	This command is used to set the duration of the Row overlap/SEG Hiz Period period.(DEFAULT=00H)
	0	1	0	row_overlap[7:0]								
34. Pre-charge VSEGH Level control (DDH)	0	1	0	1	1	0	1	1	1	0	1	This command is to set the SEG signals pad configuration to match the OLED panel hardware layout. (DEFAULT = 0FH)
	0	1	0	*	*	*	A4	A3	A2	A1	A0	
35.Read-Modify-Write (E0H)	0	1	0	1	1	1	0	0	0	0	0	Read-Modify-Write start.
36. End (EEH)	0	1	0	1	1	1	0	1	1	1	0	Read-Modify-Write end.
37. NOP (E3H)	0	1	0	1	1	1	0	0	0	1	1	Non-Operation Command
38. Write Display Data	1	1	0	Write RAM data								
39. Read Status	0	0	1	BUSY	ON/ OFF	IC ID						
40. Read Display Data	1	0	1	Read RAM data								
41. Read Panel ID (E1H)	0	1	0	1	1	1	0	0	0	0	1	
	0	1	0	*	*	*	*	*	*	Read Panel ID[1:0]		
42. Set CMD Protection(FDH)	0	1	0	1	1	1	0	0	0	0	1	This command is used to prohibit the command and memory access to avoid the noise until to disable this function. (DEFAULT= 2AH.52H)
	0	1	0	0	0	1	0	1	0	1	0	
	0	1	0	0	1	0	1	0	0	1	0	
43. DVDD Regulator Enable CMD (99H)	0	1	0	1	0	0	1	1	0	0	1	When VDD <1.98V & DVDD_EN pin is high, writing this CMD to turn off the DVDD regulator circuit for avoiding more static current generated on VDD. (DEFAULT = 00H, 00H, 00H)
	0	1	0	DVDD_REG_EN1[7:0]								
	0	1	0	DVDD_REG_EN2[7:0]								
	0	1	0	DVDD_REG_EN3[7:0]								
44. Sram read cmd in SPI&I2C(5AH)	0	1	0	0	1	0	1	1	0	1	0	Read sram cmd in SPI&I2C.
	1	0	1	rd_sram_data								
45. Set SRAM power (DEH)	0	1	0	1	1	0	1	1	1	1	0	Set SRAM power. (DEFAULT = 11H)

	0	1	0	*	*	*	A4	*	*	*	A0	
46.SPI_read data output mode (92H)	0	1	0	1	0	0	1	0	0	1	0	DEFAULT = 00H
	0	1	0	spi_dout_sel[7:0]								
47. Read IC ID (E2H)	0	1	0	1	1	1	0	0	0	1	0	DEFAULT = 60H
	0	1	0	BUSY	ON/ OFF	IC ID						

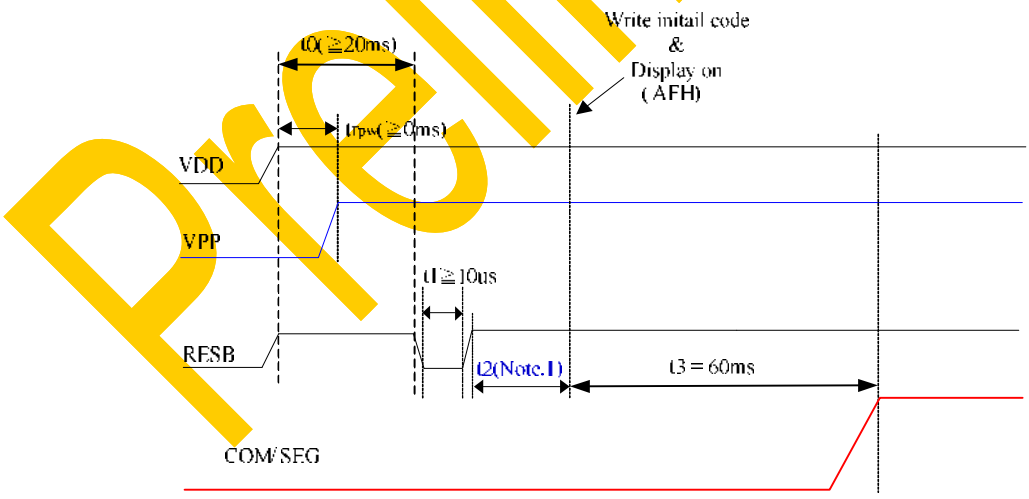
Note: Do not use any other command, or the system malfunction may result.

9. Power On/Off and Initialization

9.1. External power is being used immediately after turning on the power:

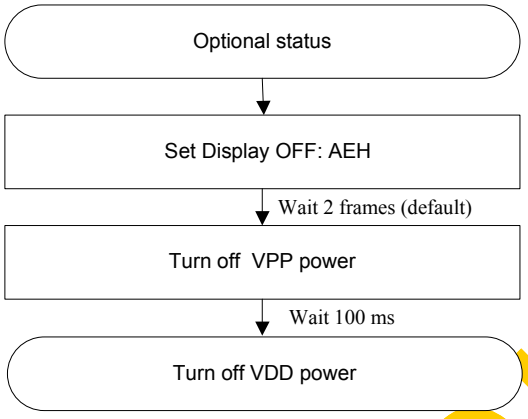


9.2. Power on sequence：

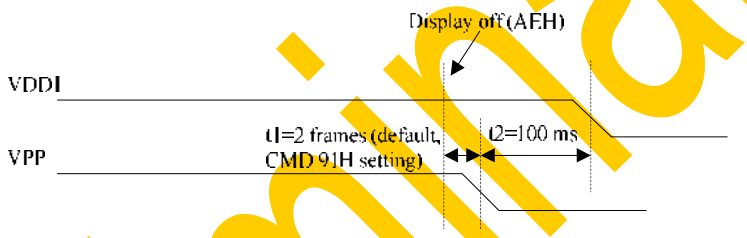


Note. It is necessary to do hardware reset in power on sequence.
Note.1 the delay time t2 is needed 2us.

9.3. Power Off



9.4. Power off sequence：



Note：There will be no damages to the display driver if the power sequences are not met.

10. Absolute Maximum Rating*

DC Supply Voltage (V_{DD}) . . . .-0.3V to +3.5V

DC Supply Voltage (V_{PP}) . . . . . -0.3V to +15V

Input Voltage . . . . . -0.3V to V_{DD} + 0.3V

Operating Ambient Temperature . . . . . -40°C to +85°C

Storage Temperature . . . . . -55°C to +125°C

10.1. Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device under these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

11. Electrical Characteristics

11.1. DC Characteristics (GND = 0V, VDD = 1.65 – 3.5V, TA =+25°C, unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{DD}	Operating voltage	1.65	-	3.5	V	
V_{PP}	OLED Operating voltage	8	-	15	V	
I_{DD}	Dynamic current consumption 1(in V_{DD})	-	-	600	μA	V_{DD} = 2.5V , I_{REF} = -18.75μA, Contrast α = 256, Display ON, display data = All ON
$I_{SP\_}$ V_{DD}	Sleep mode current consumption in VDD after hardware reset (DVDD regulator off & OSC off) (Note.1)	-	-	10	μA	During sleep, T_A = +25°C, V_{DD} = 1.65~2V, sram power off (CMD DEH bit0 & bit4 = 0)
	Sleep mode current consumption in VDD after hardware reset (DVDD regulator on & OSC off) (Note.1)	-	-	15	μA	During sleep, T_A = +25°C, V_{DD} = 2~3.5V, sram power off (CMD DEH bit0 & bit4 = 0)
$I_{SP\_}$ V_{PP}	Sleep mode current consumption in V_{PP}	-	-	5	μA	During sleep, T_A = +25°C, V_{PP} = 15V (External)
I_{PP}	OLED dynamic current consumption	-	-	1270	μA	V_{DD} = 1.8V ,V_{PP} = 15V, IREF = -18.75μA, Contrast α = 256, Display ON, Display data = All ON, No panel attached
I_{SEG}	Segment output current (External & Internal iref resistor)	540	600	660	μA	V_{DD} = 1.8V, V_{PP} = 15V, I_{REF} = -18.75μA , R_{LOAD} = 16k , Display ON. Contrast α = 256.(No panel attached)
		371	412.5	453	μA	V_{DD} = 1.8V, V_{PP} = 15V, I_{REF} = -18.75μA , R_{LOAD} = 16k , Display ON. Contrast α = 176. (No panel attached)
		270	300	330	μA	V_{DD} = 1.8V, V_{PP} = 15V, I_{REF} = -18.75μA , R_{LOAD} = 16k , Display ON. Contrast α = 128. (No panel attached)
		202	225.5	248	μA	V_{DD} = 1.8V, V_{PP} = 15V, I_{REF} = -18.75μA , R_{LOAD} = 16k , Display ON. Contrast α = 96. (No panel attached)
		33.75	37.5	41.25	μA	V_{DD} = 1.8V, V_{PP} = 15V, I_{REF} = -18.75μA , R_{LOAD} = 16k , Display ON. Contrast α = 16(No panel attached)
ΔI_{SEG1}	Segment output current uniformity	-	-	±3	%	ΔI_{SEG1} = (I_{SEG} - I_{MID})/I_{MID} X 100% I_{MID} = (I_{MAX} + I_{MIN})/2 I_{SEG} [0:159] at contrast α = 128.
ΔI_{SEG2}	Adjacent segment output current uniformity	-	-	±2	%	ΔI_{SEG2} = (I_{SEG} [N] - I_{SEG} [N+1])/(I_{SEG} [N] + I_{SEG} [N+1]) X 100% I_{SEG} [0:159] at contrast α = 128.

Note.1 Segment output current setting: I_{SEG} = α/256 X I_{REF} X scale factor

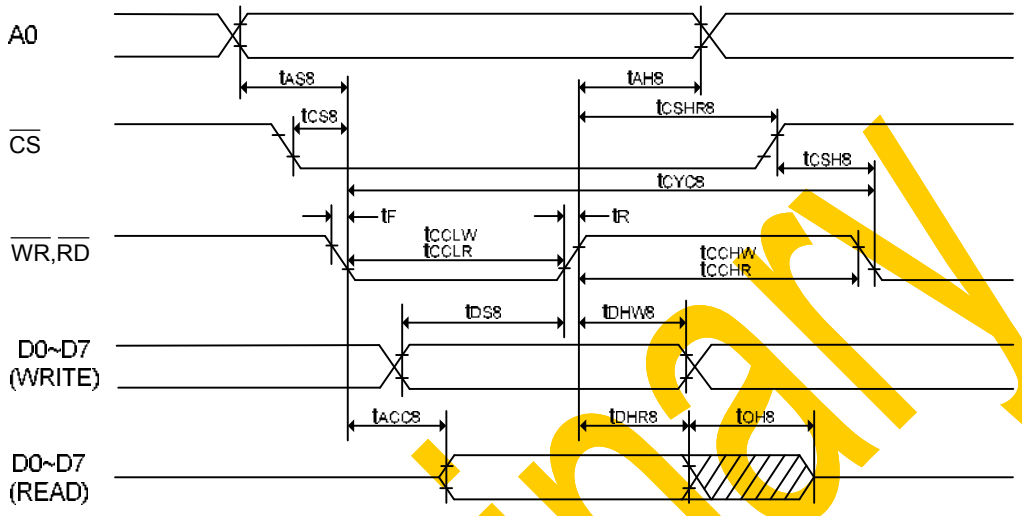
Where: α is contrast step (α=contrast+1); I_{REF} is reference current equals 18.75μA; Scale factor = 32

11.2. DC Characteristics (Continued)

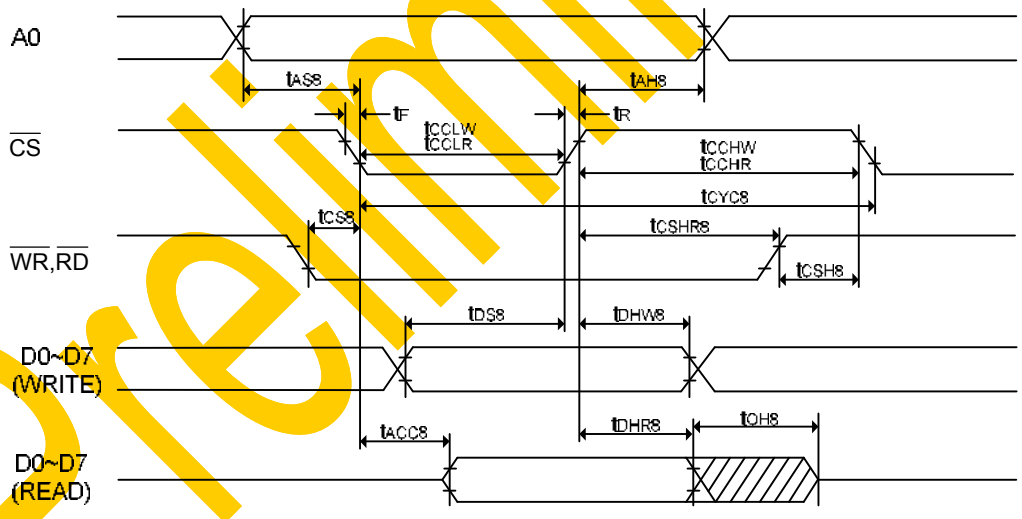
Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{IHC}	High-level input voltage	0.8 X V_{DD}	-	V_{DD}	V	A0, D0 - D7, $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$), $\overline{CS}$, CLS, CL, IM0~2 and $\overline{RES}$.
V_{ILC}	Low-level input voltage	GND	-	0.2 X V_{DD}	V	
V_{OHC}	High-level output voltage	0.8 X V_{DD}	-	V_{DD}	V	I_{OH} = -0.5mA (D0 - D7, and CL).
V_{OLC}	Low -level output voltage	GND	-	0.2 X V_{DD}	V	I_{OL} = 0.5mA (D0, D2 - D7, and CL)
V_{OLCS}	SDA low -level output voltage	GND	-	0.2 X V_{DD}	V	VDD<2V, I_{OL}=2mA (SDA)
				0.4		VDD>2V, I_{OL}=3mA (SDA)
I_{LI}	Input leakage current	-1.0	-	1.0	μA	V_{IN} = V_{DD} or GND (A0, $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$), $\overline{CS}$, CLS, IM0~2 and $\overline{RES}$).
I_{Hz}	Hz leakage current	-1.0	-	1.0	μA	When the D0 - D7, and CL are in high impedance.
f_{OSC}	Oscillation frequency	4.1	4.4	4.7	MHz	T_A = +25°C.
f_{FRM}	Frame frequency for 160 Commons	98	105	112	Hz	When fosc = 4.4MHz, Divide ratio =2, display width = 135 DCLKs.
R_{ON1}	Common switch resistance	10	15	35	Ω	V_{pp}=15V, V_{com}= GND +0.4V

11.3. AC Characteristics

11.3.1. System buses Read/Write characteristics 1 (For the 8080 Series Interface MPU)



8080-series parallel interface cycle (Form1)

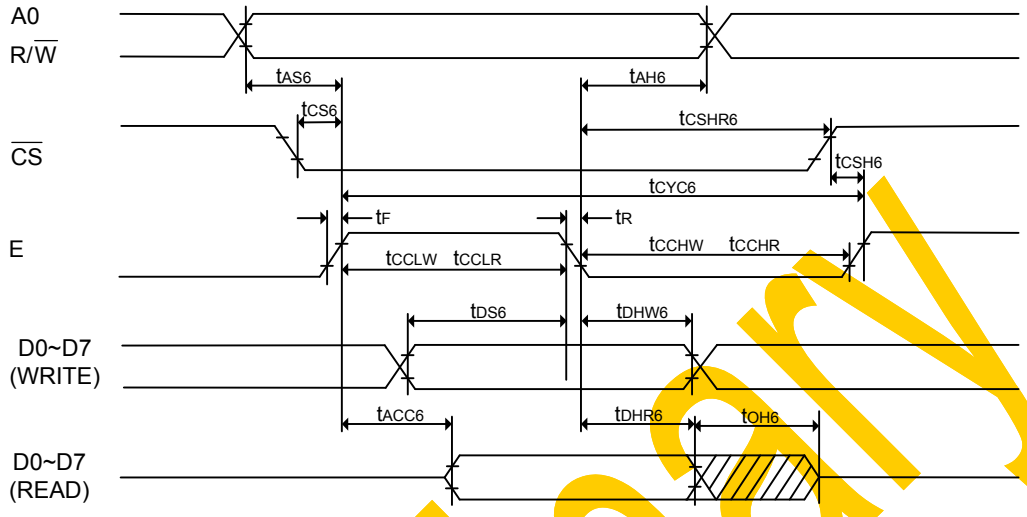


8080-series parallel interface cycle (Form2)

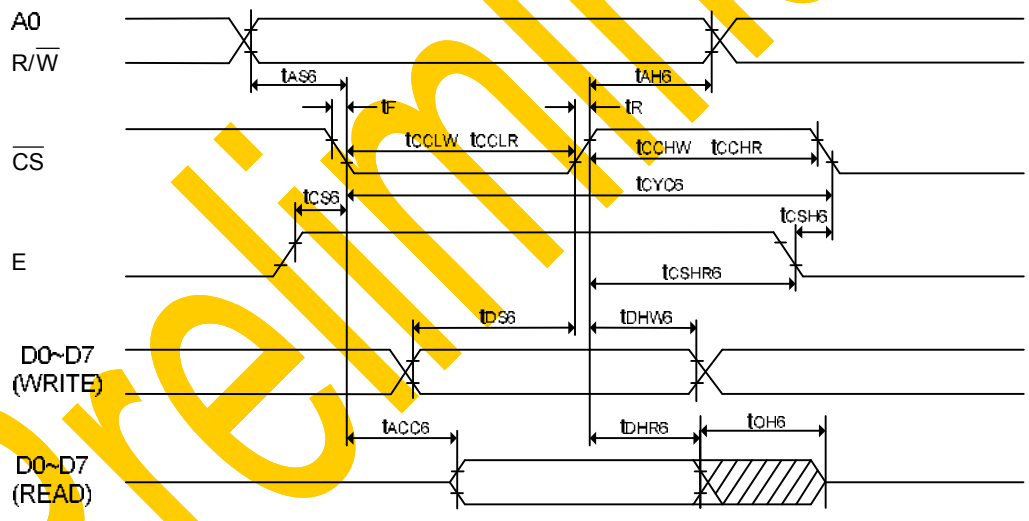
(VDD = 1.65 – 3.5V, T_A = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{CYC8}	System cycle time	300	-	-	ns	
t_{AS8}	Address setup time	0	-	-	ns	
t_{AH8}	Address hold time	0	-	-	ns	
t_{DS8}	Data setup time	40	-	-	ns	
t_{DHW8}	Write Data hold time	10	-	-	ns	
t_{DHR8}	Read Data hold time	10	-	-	ns	
t_{OH8}	Output disable time	-	-	70	ns	C_L = 100pF
t_{ACC8}	$\overline{RD}$ access time	-	-	140	ns	C_L = 100pF
t_{CCLW}	Control L pulse width (WR)	150	-	-	ns	
t_{CCLR}	Control L pulse width (RD)	150	-	-	ns	
t_{CCHW}	Control H pulse width (WR)	150	-	-	ns	
t_{CCHR}	Control H pulse width (RD)	150	-	-	ns	
t_R	Rise time	-	-	15	ns	
t_F	Fall time	-	-	15	ns	
t_{CS8}	Chip select setup time	0	-	-	ns	
t_{CSH8}	Chip select hold time	20	-	-	ns	
t_{CSHR8}	Chip select hold time to read signal	20	-	-	ns	

11.3.2. System buses Read/Write Characteristics 2 (For the 6800 Series Interface MPU)



6800-series parallel interface cycle (Form1)

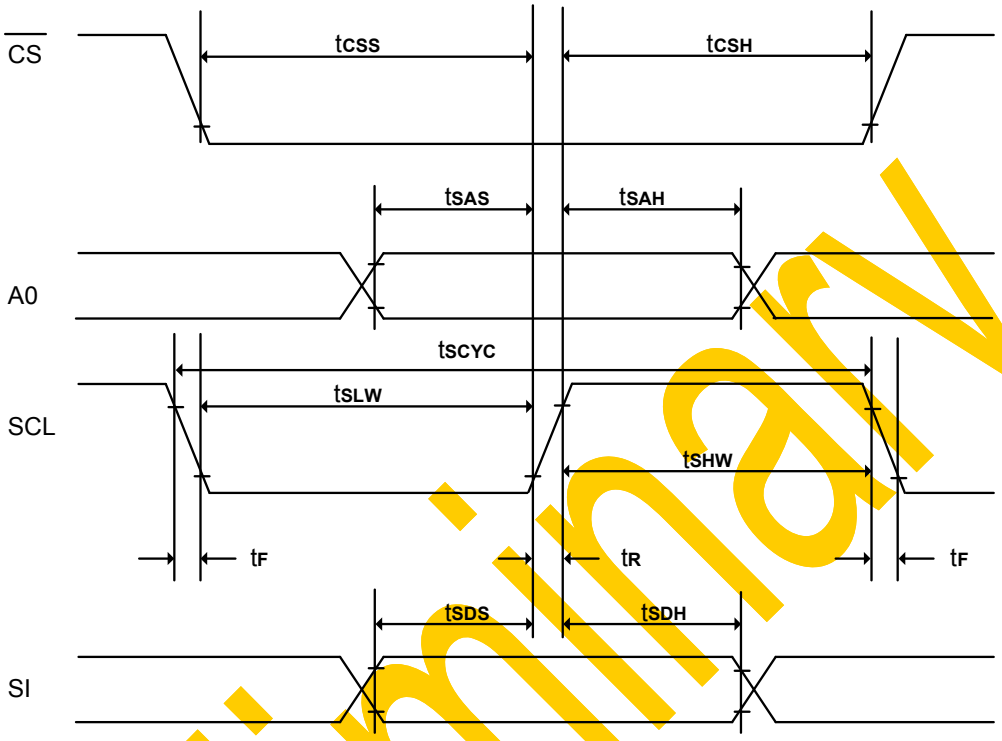


6800-series parallel interface cycle (Form2)

(VDD = 1.65 – 3.5V, T_A = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{CYC6}	System cycle time	300	-	-	ns	
t_{AS6}	Address setup time	0	-	-	ns	
t_{AH6}	Address hold time	0	-	-	ns	
t_{DS6}	Data setup time	40	-	-	ns	
t_{DHW6}	Write Data hold time	10	-	-	ns	
t_{DHR6}	Read Data hold time	10	-	-	ns	
t_{OH6}	Output disable time	-	-	70	ns	C_L = 100pF
t_{ACC6}	Access time	-	-	140	ns	C_L = 100pF
t_{EWHW}	Enable H pulse width (Write)	150	-	-	ns	
t_{EWHR}	Enable H pulse width (Read)	150	-	-	ns	
t_{EWLW}	Enable L pulse width (Write)	150	-	-	ns	
t_{EWLR}	Enable L pulse width (Read)	150	-	-	ns	
t_R	Rise time	-	-	15	ns	
t_F	Fall time	-	-	15	ns	
t_{CS6}	Chip select setup time	0	-	-	ns	
t_{CSH6}	Chip select hold time	20	-	-	ns	
t_{CSHR6}	Chip select hold time to read signal	20	-	-	ns	

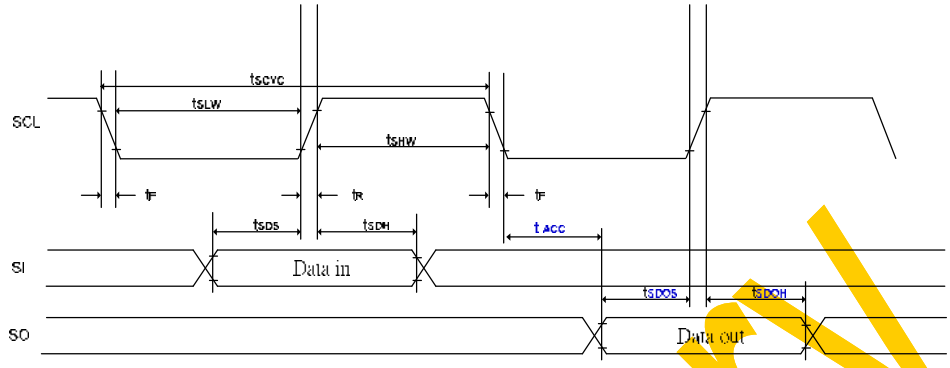
11.3.3. System buses Write characteristics 3 (For 4 wire SPI)



(VDD = 1.65 – 3.5V, T_A = +25°C)

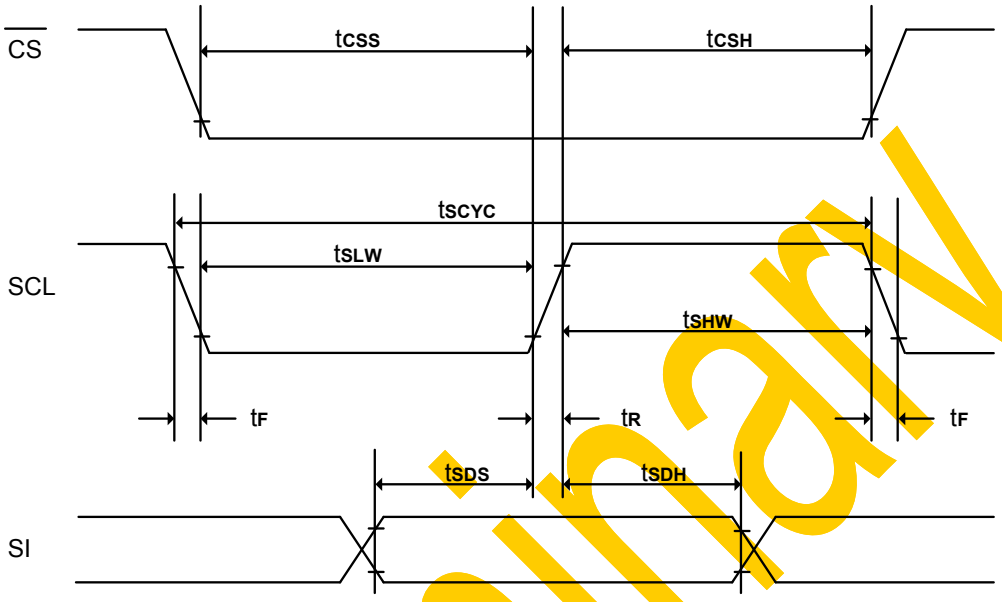
Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
tSCYC	Serial clock cycle	50	-	-	ns	
tSAS	Address setup time	30	-	-	ns	
tSAH	Address hold time	30	-	-	ns	
tSDS	Data setup time	20	-	-	ns	
tSDH	Data hold time	20	-	-	ns	
tCSS	$\overline{CS}$ setup time	45	-	-	ns	
tCSH	$\overline{CS}$ hold time time	12	-	-	ns	
tSHW	Serial clock H pulse width	20	-	-	ns	
tSLW	Serial clock L pulse width	20	-	-	ns	
tR	Rise time	-	-	3	ns	
tF	Fall time	-	-	3	ns	

11.3.3.1. System buses Read characteristics 3 (For 4 wire SPI)



Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
tSCYC	Serial clock cycle	50	-	-	ns	There's delay time between every byte data. (Format 1)
tSCYC	Serial clock cycle	200	-	-	ns	There's no delay time between every byte data. (Format 2)
tACC	Access time	10	-	-	ns	
tSDOS	Address setup time	10	-	-	ns	
tSDOH	Address hold time	10	-	-	ns	

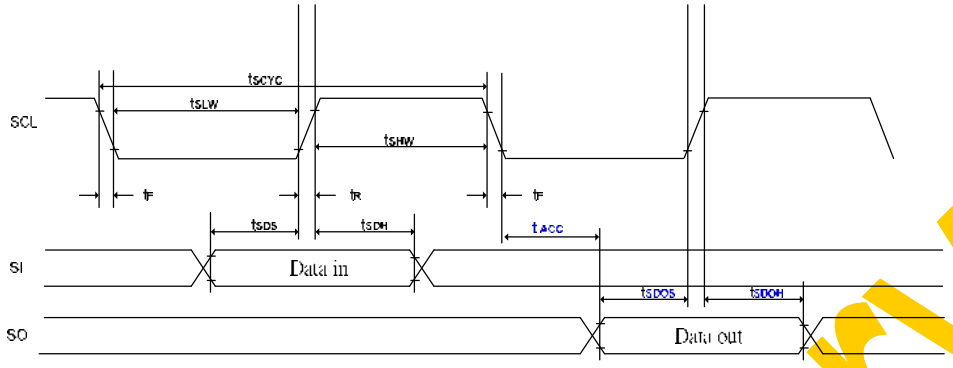
11.3.4. System buses Write characteristics 4(For 3 wire SPI)



(VDD = 1.65 – 3.5V, TA = +25°C)

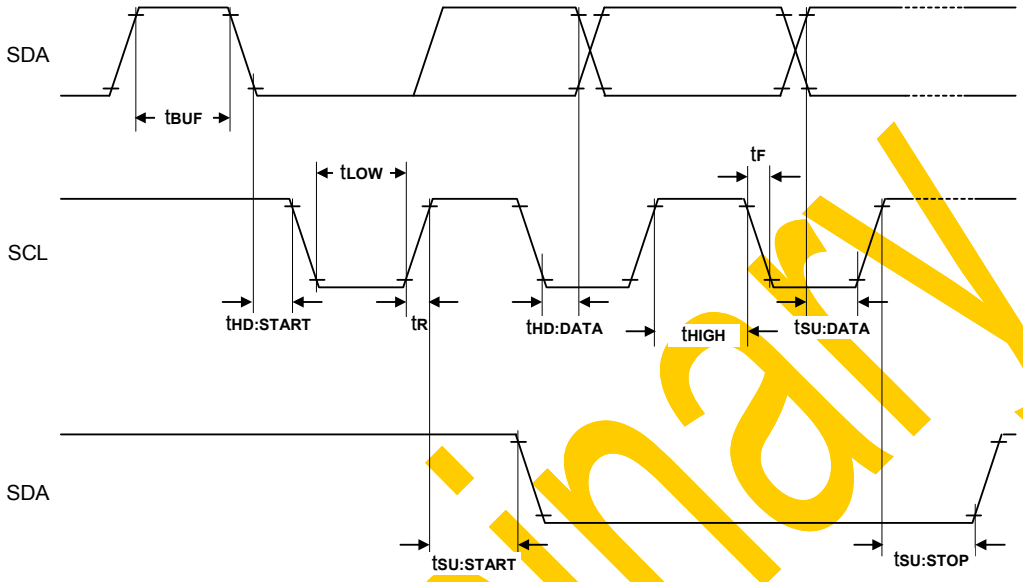
Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
tSCYC	Serial clock cycle	50	-	-	ns	
tSDS	Data setup time	20	-	-	ns	
tSDH	Data hold time	20	-	-	ns	
tCSS	$\overline{CS}$ setup time	45	-	-	ns	
tCSH	$\overline{CS}$ hold time time	12	-	-	ns	
tSHW	Serial clock H pulse width	20	-	-	ns	
tSLW	Serial clock L pulse width	20	-	-	ns	
tR	Rise time	-	-	3	ns	
tF	Fall time	-	-	3	ns	

11.3.4.1. System buses Read characteristics 4 (For 3 wire SPI)



Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
tSCYC	Serial clock cycle	50	-	-	ns	There's delay time between every byte data. (Format 1)
tSCYC	Serial clock cycle	200	-	-	ns	There's no delay time between every byte data. (Format 2)
tACC	Access time	10	-	-	ns	
tSDOS	Address setup time	10	-	-	ns	
tSDOH	Address hold time	10	-	-	ns	

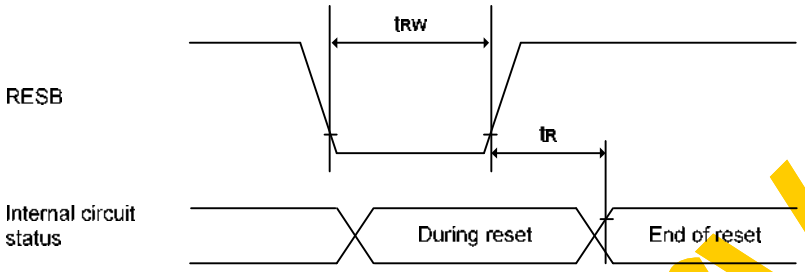
11.3.5. I²C interface characteristics



(VDD = 1.65 – 3.5V, TA = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
fSCL	SCL clock frequency	DC	-	400	kHz	
TLOW	SCL clock Low pulse width	1.3	-	-	us	
THIGH	SCL clock H pulse width	0.6	-	-	us	
TSU:DATA	data setup time	100	-	-	ns	
THD:DATA	data hold time	0	-	0.9	us	
TR	SCL、SDA rise time	20+0.1Cb	-	300	ns	
TF	SCL、SDA fall time	20+0.1Cb	-	300	ns	
Cb	Capacity load on each bus line	-	-	400	pF	
TSU:START	Setup timefor re-START	0.6	-	-	us	
THD:START	START Hold time	0.6	-	-	us	
TSU:STOP	Setup time for STOP	0.6	-	-	us	
TBUF	Bus free times between STOP and START condition	1.3	-	-	us	

11.3.6. Reset Timing



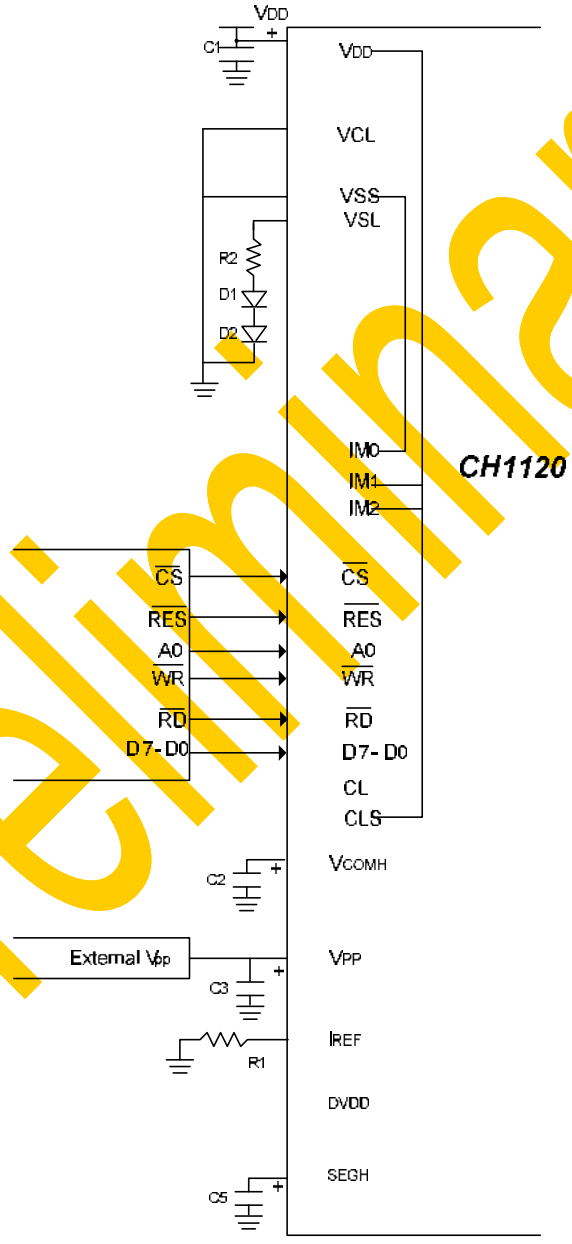
(VDD = 1.65 – 3.5V, TA = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
tR	Reset time	-	-	2.0	us	
tRW	Reset low pulse width	10.0	-	-	us	

12. Application Circuit (for reference only)

12.1. Reference Connection to MPU:

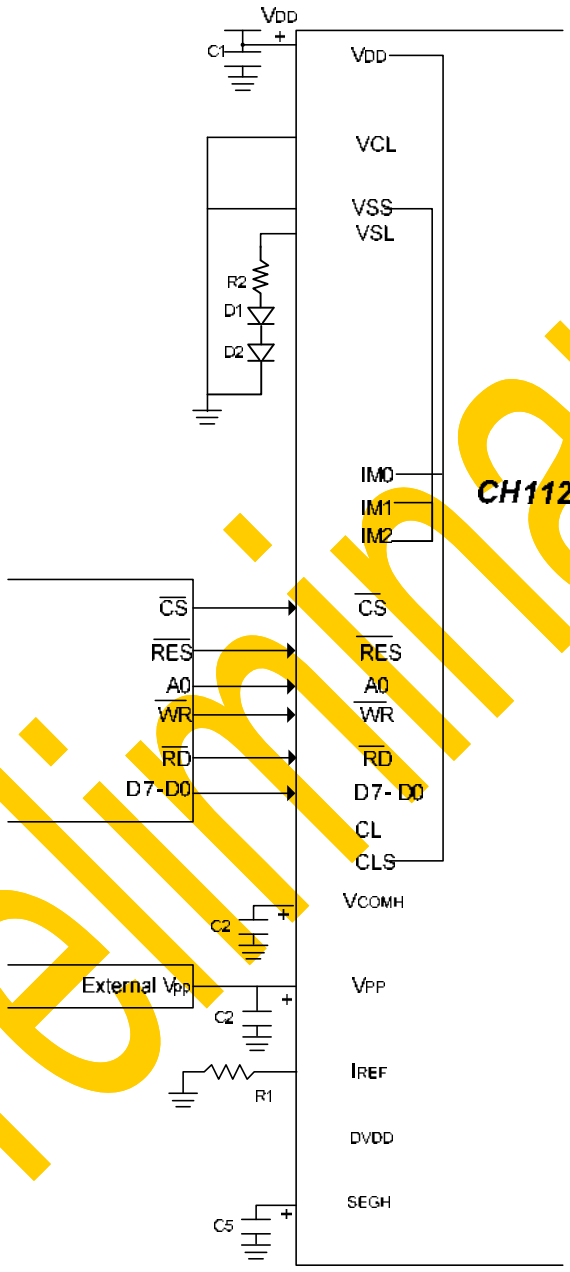
12.1.1. 8080 series interface: (Internal oscillator, External Vpp)



Note:

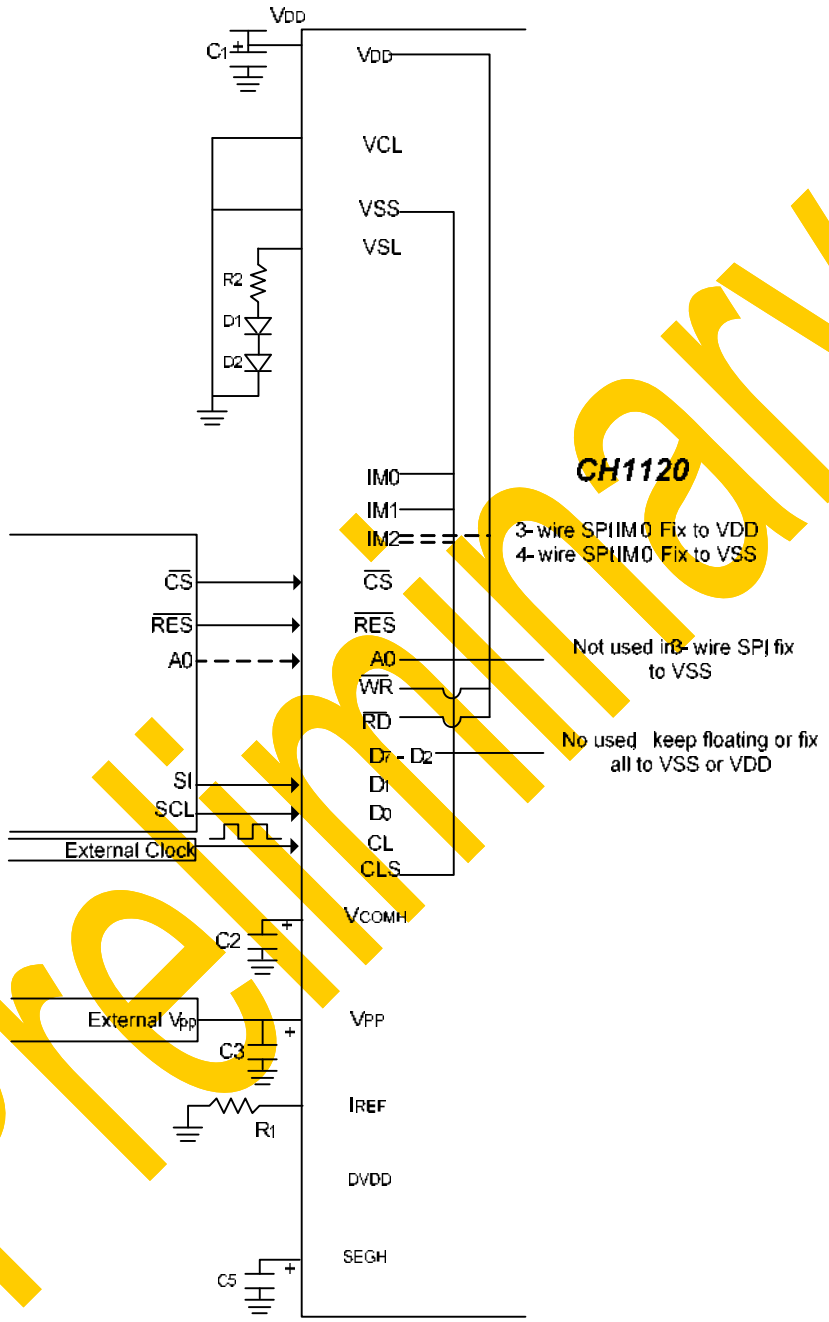
C1---C5: 4.7μF
R_1: about 750K (Refer to the table 8), R_1 = (Voltage at I_{REF} – GND)/I_{REF}
R2: Recommend **50Ω**
A capacitor should be connected between DVDD and GND if necessary.

12.1.2. 6800 Series Interface: (Internal oscillator, External Vpp)



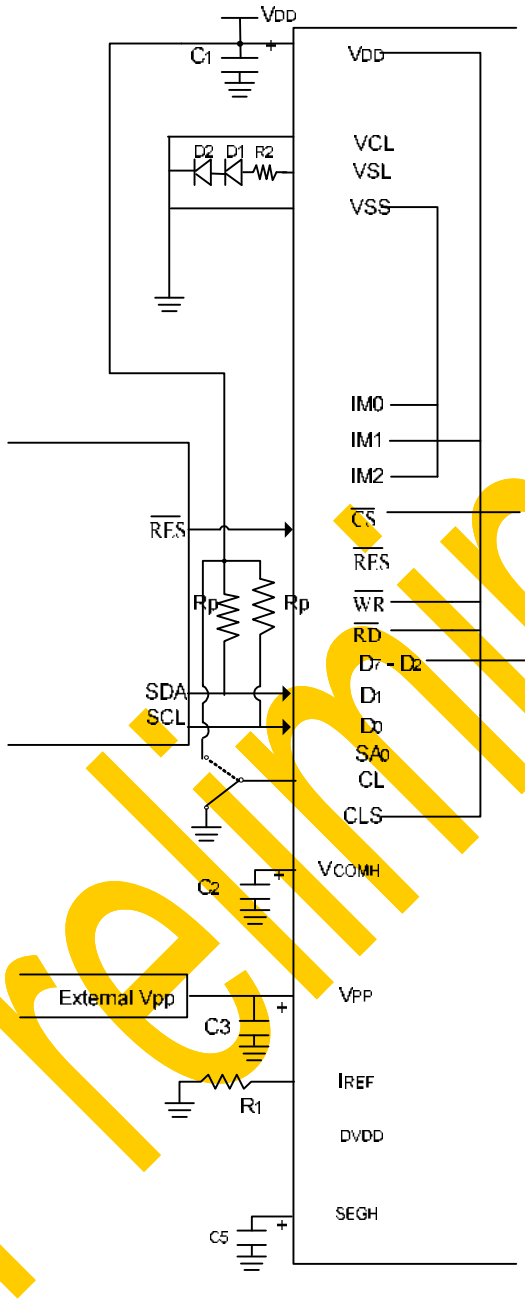
Note:
C1---C5: 4.7μF
R_1: about 750K (Refer to the table 8), R_1 = (Voltage at I_{REF} – GND)/I_{REF}
R2: Recommend 50Ω
A capacitor should be connected between DVDD and GND if necessary.

12.1.3. Serial Interface (3-wire or 4-wire SPI): (External oscillator, External VPP, Max 15V)



Note:
C1---C5: 4.7μF
R1: Recommend 750K (Refer to the table 8)
R2: Recommend 50Ω
A capacitor should be connected between DVDD and GND if necessary.

12.1.4. I²C Interface (Internal oscillator, External VPP, Max 15V)



Note:
C1---C5:4.7μF
R1: Recommend 750K (Refer to the table 8)
R2: Recommend 50Ω
The least significant bit of the slave address is set by connecting the input SA0 to either logic 0(GND) or 1(VDD)
The positive supply of pull-up resistor must equal to the value of VDD
Recommend the value of resistor Rp equal to 1.5KΩ
A capacitor should be connected between DVDD and GND if necessary.

13. Ordering Information

Part No.	Package
CH1120	Gold bump on chip tray

14. SPEC Revision History

Version	Content	Date
0.0	Original	AUG.2018
0.1	1. Add VPP.VSS.VCL.VSL pad description – P.3 2. Modify figure 4 wire SPI format 2 (CMD Read) – P.19 3. Modify figure 3 wire SPI format 2 (CMD Read) – P.22 4. Modify 1 column/row scroll sample code. – P.50~P.51 5. Remove cascade function. 6. Remove I2C read ram function.	June.2019
0.2	1. Modify D5h - divide ratio – P.68 2. Modify 93H - Set Dis-charge Period – P.69 3. Modify Fosc & $f_{FRM\ condition}$ – P.88	Jan.2020
0.3	1. Add D8H - Dis-charge_back Period– P.69 2. Modify the picture of discharge/precharge-P70	Jun.2020
0.4	1. Modify the protocol of 4-wire SPI read CMD and SRAM P19-21 2. Modify the protocol of 3-wire SPI read CMD and SRAM P23-26 3. Add 92H SPI_read data output mode P84	Jun.2020
0.5	1. Add note2 When using SPI read SRAM P21&26 2. Add a note of read sram in Mono mode P81 3. Add the speed of 4-wire&3-wire SPI read SRAM P99&P101 4. Modify the description of tACC P99&P101 5. Modify the application circuit about DVDD P104-107	Aug.2020
0.6	1. Modify Mono mode register setting. – P.38 2. Add note2 to B8H – Set grayscale table. – P.68 3. Add condition to SPI read characteristic. – P.99 & P.101 4. Add Read IC ID register (E2H) . – P.84 & P.89	Oct.2020
0.7	1. Change display module to display driver. – P.91	Mar.2021
0.8	1. Modifiy the timming of t_{SCYC} in the 3-SPI/4-SPI sequence diagram.-P.98-101	Apr.2021

0.9	1. Modify the table of oscillator frequency setting. - P.71-72 2. Add the range of fOSC and fFRM. -P.93 3. Delete the 60us delay in the Power on sequence -P.90	Aug.2021